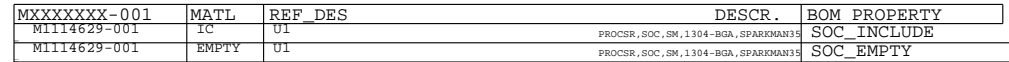
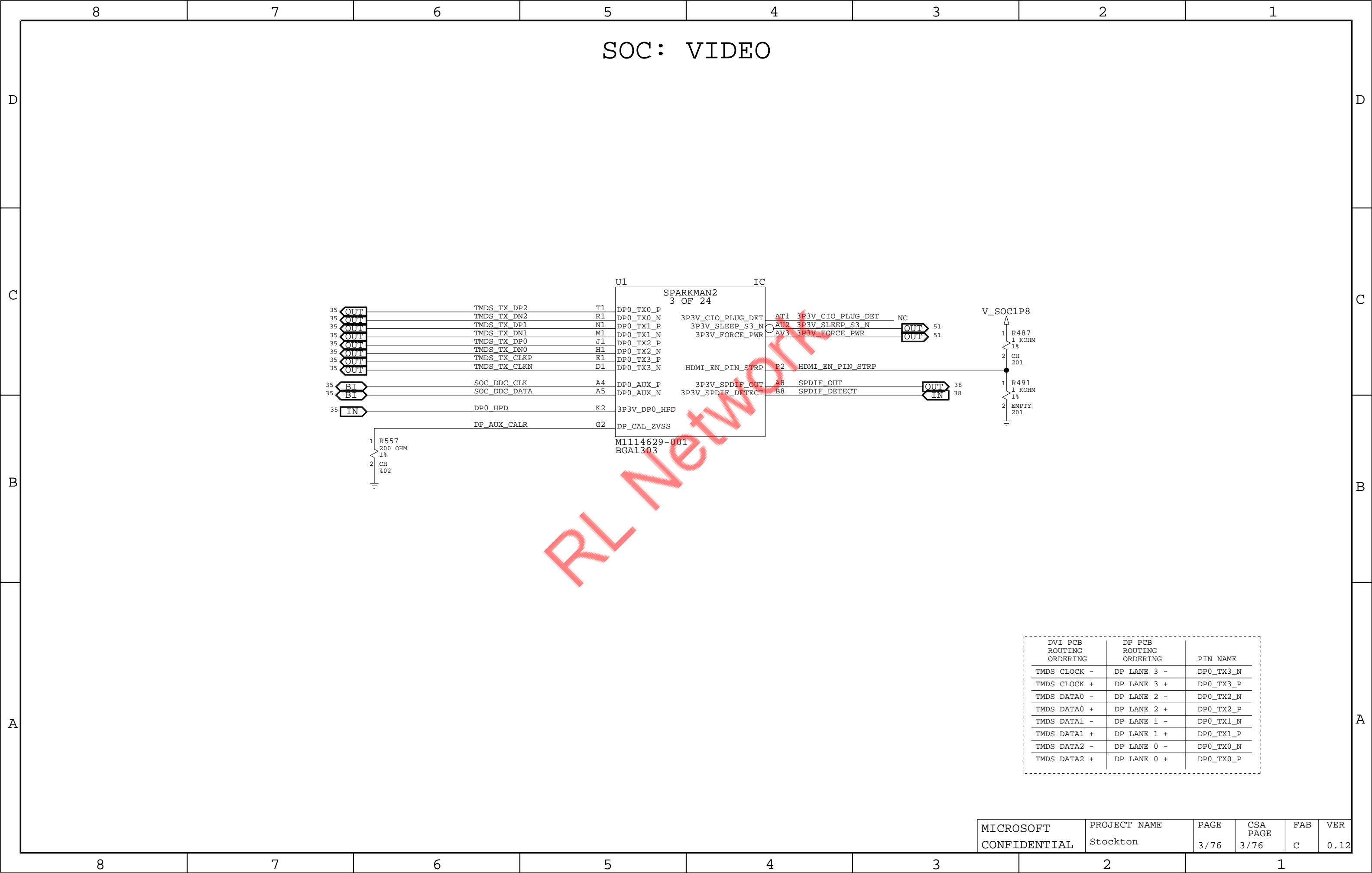


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D	SHEET	SHEET NAME			SHEET	SHEET NAME			STOCKTON FAB C REV 0.12						
	1	NONE			41	CONN: M.2									
	2	SOC: PCIEX,CLOCKS			42	CONN: ODD									
	3	SOC: VIDEO			43	CONN: FRONT PANEL, FAN, NEXUS									
	4	SOC POWER: MEMIO, CPUCORE, SOC			44	CONN: POWER									
	5	SOC: POWER: GFXCORE, MEMPHY, MISC			45	VREGS: V_12P0_GATED									
	6	SOC: POWER: VSS			46	VREGS: INPUT DECOUPLING									
	7	SOC: POWER: VSS			47	VREGS: V_CPUCORE, V_GFXCORE CONTROLLER									
C	8	SOC: DEBUG, SB SIGNALS, V_BAT, VOLTAGE SENSE			48	VREGS: V_GFXCORE OUTPUT PHASE 1 & 2			C						
	9	SOC: V_GFXCORE DECOUPLING			49	VREGS: V_GFXCORE OUTPUT PHASE 3 & 4									
	10	SOC: V_SOC DECOUPLING			50	VREGS: V_CPUCORE OUTPUT									
	11	SOC: V_MEMIO/V_MEMPHY DECOUPLING			51	VREGS: V_MEMIO, V_MEMPHY, V_SOC CONTROLLER									
	12	SOC: V_CPUCORE DECOUPLING			52	VREGS: V_MEMIO, V_MEMPHY, V_SOC SENSE									
	13	SOC & Memory: CHA/PHY0			53	VREGS: V_MEMIO AND V_MEMPHY OUTPUT									
	14	MEMORY: PWR/VSS & DECAP, A			54	VREGS: V_SOC OUTPUT									
	15	SOC & Memory: CHB/PHY1			55	VREGS: V_5P0									
B	16	MEMORY: PWR/VSS & DECAP, B			56	VREGS: V_SOC1P8, V_DRAM1P8			B						
	17	SOC & Memory: CHC/PHY2			57	VREGS: V_SOCPHY, V_FUSE									
	18	MEMORY: PWR/VSS & DECAP, C			58	VREGS: V_SB1P8, V_SB1P1									
	19	SOC & Memory: CHD/PHY3			59	VREGS: V_3P3STBY									
	20	MEMORY: PWR/VSS & DECAP, D			60	VREGS: V_3P3_GATED, V_3P3_CFX									
	21	SB: SMC			61	VREGS: V_1P1STBY, V_1P8STBY									
	22	SB: USB			62	I2C									
	23	SB: PCIEX, SATA, VIDEO			63	DEBUG: MARGIN V_SOCPHY,V_SOC1P8, V_DRAM1P8									
A	24	SB: SMM UART, SPI, JTAG, GPIO			64	DEBUG: MONITOR V_SOC1P8, V_SOCPHY, V_12P0, V_DRAM1P8			A						
	25	SB: POWER (VSS)			65	DEBUG: MONITOR M.2. CFEXPRESS									
	26	SB: POWER			66	DEBUG: FACET HEADER									
	27	SB: DECOUPLING			67	DEBUG: FTDI BRIDGE									
	28	SB: CLOCKS, STRAPPING, POR			68	DEBUG: FTDI BUFF, USB, PWR									
	29	CLOCK: PCIE 100MHZ SS			69	DEBUG: SWITCHES, LEDS									
	30	CLOCK: PCIE 100MHZ NS			70	DEBUG: HDT									
	31	ETHERNET CONTROLLER			71	DEBUG: VR HEADERS, TEST POINTS, CONNECTORS									
32	SB: EMMC (LEGACY)			72	LABELS AND MOUNTING			A							
33	MEMORY: SPI FLASH SOC			73	BOM DEFINITIONS										
34	MEMORY: SPI FLASH			74	STOCKTON_NEXUS										
35	HDMI: VIDEO OUT			75	B2B CONN AND LABELS										
36	HDMI: LOAD SWITCHES			76	NEXUS LED AND POWER SWITCH										
37	AUDIO: PREMIUM AND RETAIL														
38	CONN: RJ45, SPDIF, CFEXPRESS														
39	CONN: USB (FRONT & REAR)														
40	CONN: WIFI														
RULES: (APPLIED WHEN POSSIBLE) 1. MSB TO LSB IS TOP TO BOTTOM 2. WHEN POSSIBLE: INPUTS ON LEFT, OUTPUTS ON RIGHT 3. ORDER OF PAGES=CHIP INTERFACES, TERMINATION, POWER, DECOUPLING 4. AVOID USING OFF PAGE CONNECTORS FOR ON PAGE CONNECTIONS 5. LANED SIGNALS ARE GROUPED ON SYMBOLS 6. TRANSMITTER NAME USED AS PREFIX WITH RX AND TX CONNECTIONS 7. SUFFIX V IS USED FOR VOLTAGE RAIL SIGNAL NAMES 8. SUFFIX _DP AND _DN ARE USED FOR DIFFERENTIAL PAIRS 9. UNNAMED NETS ARE NAMED WITH /2 TEXT SIZE 10.SUFFIX _N FOR ACTIVE LOW OR N JUNCTION 12.SUFFIX _P FOR P JUNCTION 13.SUFFIX _EN FOR ENABLE 14.'CLK' FOR CLOCKS, 'RST' FOR RESETS 15.PWRGD FOR POWER GOOD 16.REV AND FAB ARE SET USING CUSTOM VARIABLES TOOLS>OPTIONS>VARIABLES															
DRAWING Tue Jun 25 13:39:30 2019															
8		7		6		5		4		3		2		1	
MICROSOFT CONFIDENTIAL		PROJECT NAME Stockton		PAGE 1/76		CSA PAGE 1/76		FAB C		VER 0.12					

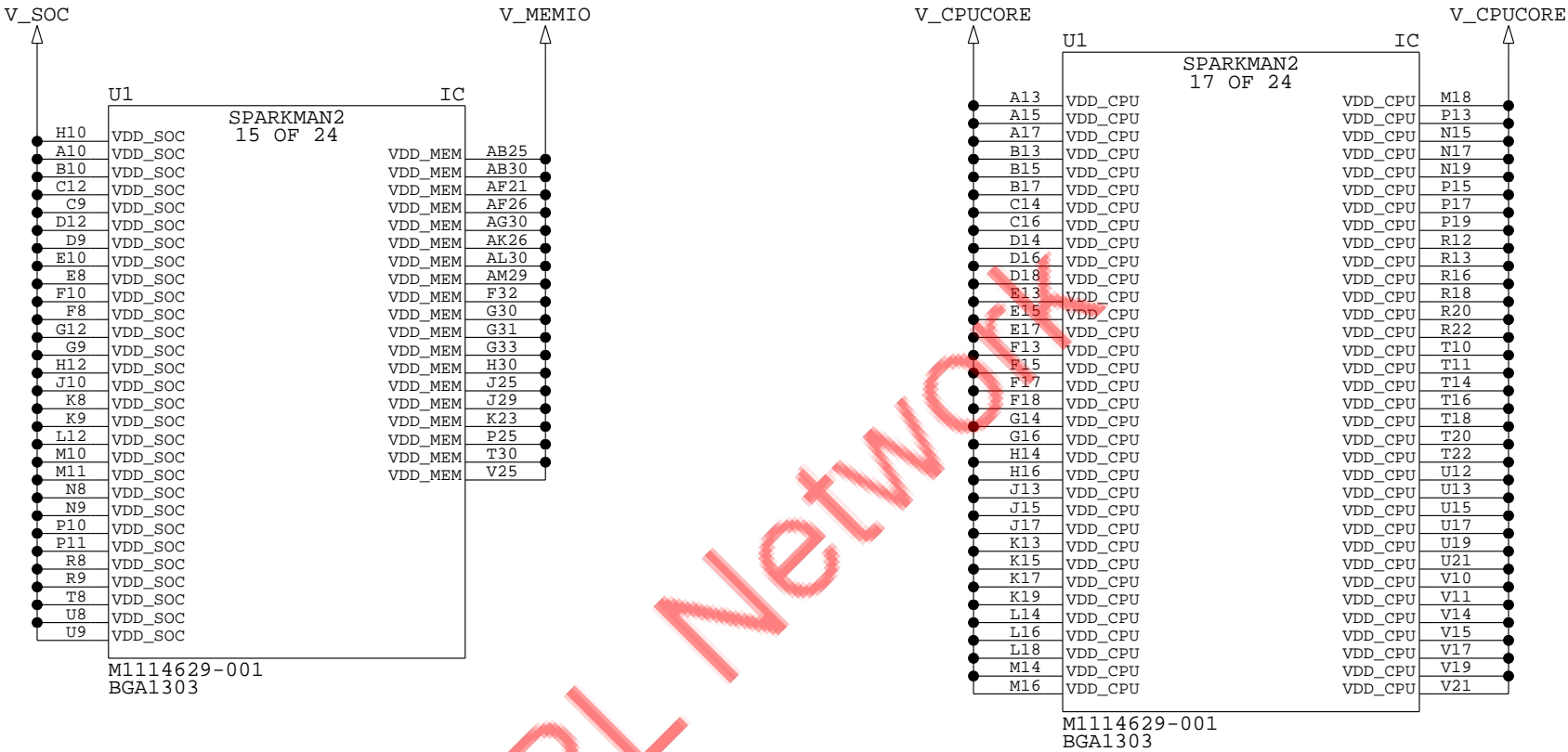
K SOC_SPARE_TP
K SOC_SPARE_TN
K SOC_ENET_TP
K SOC_ENET_TN
K L1_SOC_CFX_TP
K L1_SOC_CFX_TN
K L0_SOC_CFX_TP
K L0_SOC_CFX_TN
K L1_SOC_M2_TP
K L1_SOC_M2_TN
K L0_SOC_M2_TP
K L0_SOC_M2_TN
K L1_SOC_SB_TP
K L1_SOC_SB_TN
K L0_SOC_SB_TP
K L0_SOC_SB_TN
K CAL_VSS

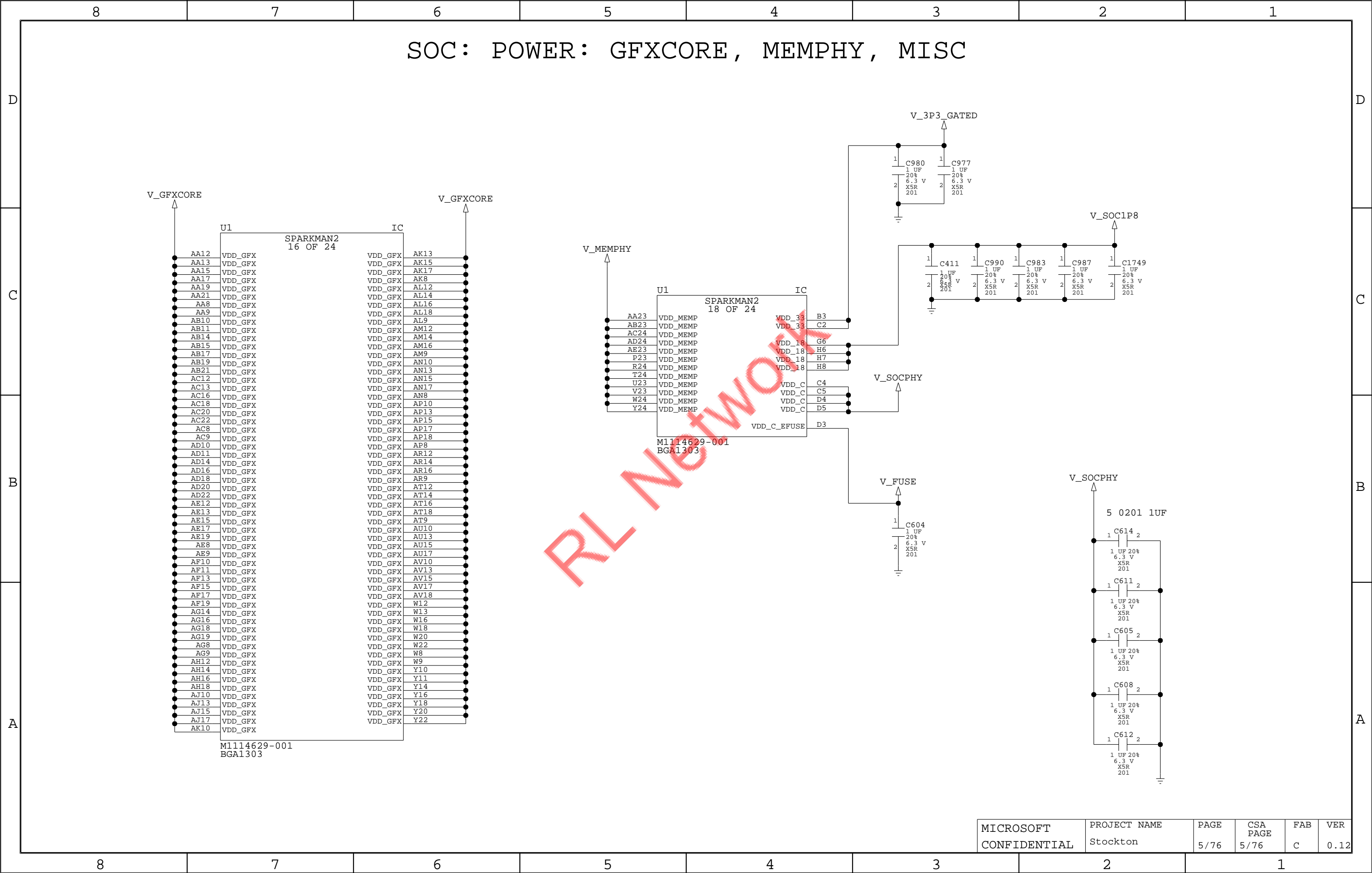
R501
200 OHM
1%
CH
402

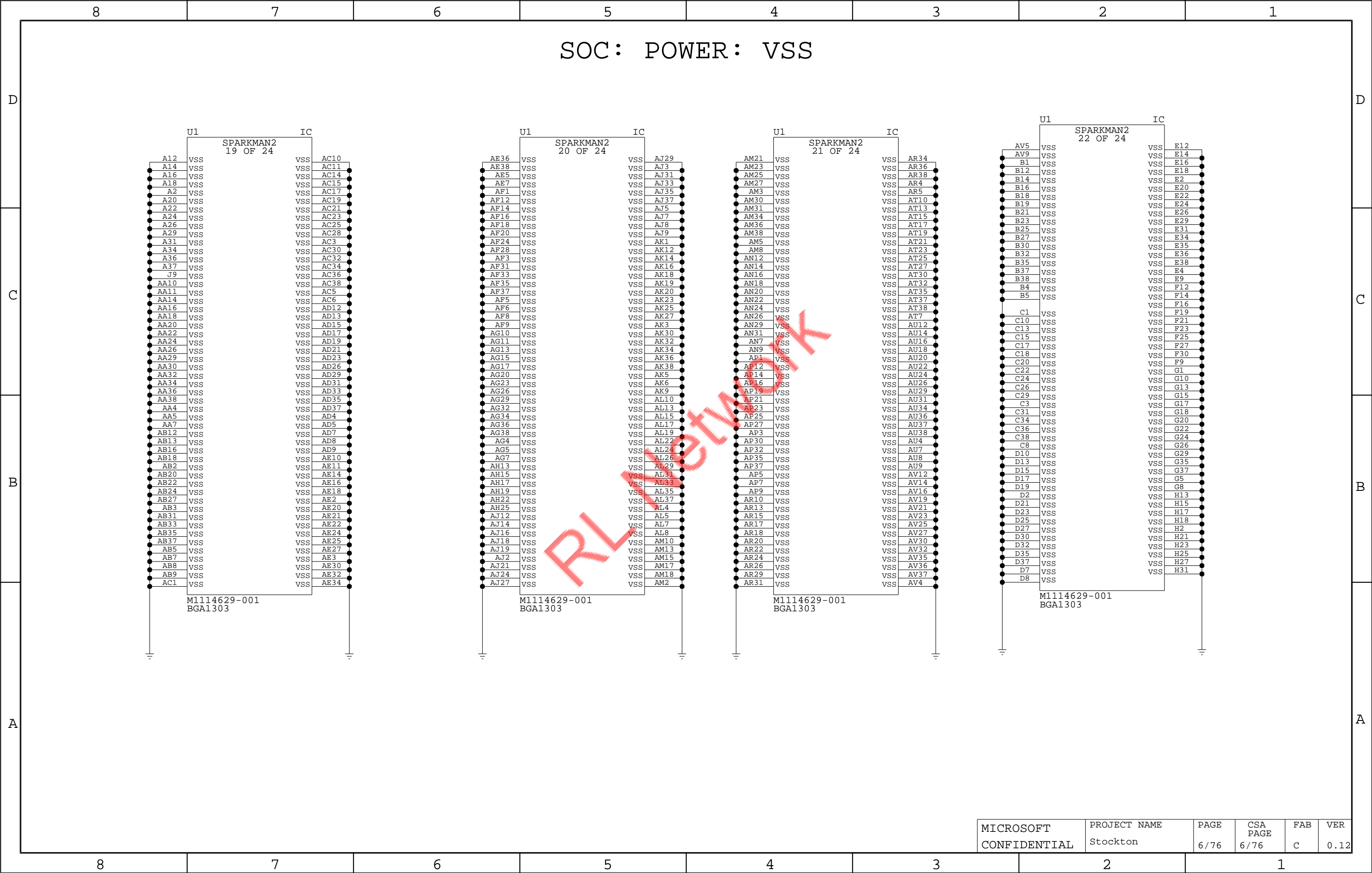




SOC POWER: MEMIO, CPUCORE, SOC







U1

SPARKMAN2

22 OF 24

IC

AV5

VSS

AV9

VSS

B1

VSS

B12

VSS

B14

VSS

B16

VSS

B18

VSS

B19

VSS

B21

VSS

B23

VSS

B25

VSS

B27

VSS

B30

VSS

B32

VSS

B35

VSS

B37

VSS

B38

VSS

B4

VSS

B5

VSS

C1

VSS

C10

VSS

C13

VSS

C15

VSS

C17

VSS

C18

VSS

C20

VSS

C22

VSS

C24

VSS

C26

VSS

C29

VSS

C3

VSS

C31

VSS

C34

VSS

C36

VSS

C38

VSS

C8

VSS

D10

VSS

D13

VSS

D15

VSS

D17

VSS

D19

VSS

D2

VSS

D21

VSS

D23

VSS

D25

VSS

D27

VSS

D30

VSS

D32

VSS

D35

VSS

D37

VSS

D7

VSS

D8

VSS

E12

VSS

E14

VSS

E16

VSS

E18

VSS

E2

VSS

E20

VSS

E22

VSS

E24

VSS

E26

VSS

E29

VSS

E31

VSS

E34

VSS

E35

VSS

E36

VSS

E38

VSS

E4

VSS

E9

VSS

F12

VSS

F14

VSS

F16

VSS

F19

VSS

F21

VSS

F23

VSS

F25

VSS

F27

VSS

F30

VSS

F9

VSS

G1

VSS

G10

VSS

G13

VSS

G15

VSS

G17

VSS

G18

VSS

G20

VSS

G22

VSS

G24

VSS

G26

VSS

G29

VSS

G35

VSS

G37

VSS

G5

VSS

G8

VSS

H13

VSS

H15

VSS

H17

VSS

H18

VSS

H2

VSS

H21

VSS

H23

VSS

H25

VSS

H27

VSS

H31

VSS

M1114629-001
BGA1303

MICROSOFT
CONFIDENTIAL

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Stockton

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FAB
C

VER
0.12

8

7

6

5

4

3

2

1

SOC: POWER: VSS

D

C

B

A

U1

IC

SPARKMAN2

23 OF 24

H33

VSS

H34

VSS

H36

VSS

H38

VSS

H5

VSS

H9

VSS

J12

VSS

J14

VSS

J16

VSS

J18

VSS

J19

VSS

J2

VSS

J22

VSS

J24

VSS

J26

VSS

J3

VSS

J30

VSS

J33

VSS

J35

VSS

J37

VSS

J6

VSS

J7

VSS

J8

VSS

K1

VSS

K10

VSS

K12

VSS

K14

VSS

K16

VSS

K18

VSS

K20

VSS

K26

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K29

VSS

K3

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K32

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K34

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K36

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K38

VSS

K6

VSS

L13

VSS

L15

VSS

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L21

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L24

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M13

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M15

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M17

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M19

VSS

M2

VSS

M20

VSS

M22

VSS

M25

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M28

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M31

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M33

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M35

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M37

VSS

M4

VSS

M5

VSS

M7

VSS

M9

VSS

N10

VSS

N11

VSS

N14

VSS

N16

VSS

N18

VSS

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VSS

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N23

VSS

N26

VSS

N27

VSS

N3

VSS

N30

VSS

N32

VSS

N34

VSS

N36

VSS

N38

VSS

N5

VSS

N7

VSS

P1

VSS

P12

VSS

P14

VSS

P16

VSS

P18

VSS

P21

VSS

P22

VSS

P24

VSS

P26

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P29

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VSS

P31

VSS

P33

VSS

P35

VSS

P37

VSS

P5

VSS

P6

VSS

P9

VSS

R10

VSS

R11

VSS

R14

VSS

R15

VSS

R17

VSS

R19

VSS

R2

VSS

R23

M1114629-001
BGA1303

U1

IC

SPARKMAN2

24 OF 24

R25

VSS

R28

VSS

R30

VSS

R32

VSS

R34

VSS

R36

VSS

R38

VSS

R4

VSS

R5

VSS

R7

VSS

T12

VSS

T13

VSS

T15

VSS

T17

VSS

T19

VSS

T2

VSS

T21

VSS

T23

VSS

T27

VSS

T3

VSS

T31

VSS

T33

VSS

T35

VSS

T37

VSS

T5

VSS

T7

VSS

T9

VSS

U1

VSS

U10

VSS

U11

VSS

U14

VSS

U16

VSS

U18

VSS

U2

VSS

U20

VSS

U22

VSS

U24

VSS

U25

VSS

U26

VSS

U29

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U3

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U30

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U32

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U34

VSS

U36

VSS

U38

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U5

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U6

VSS

V12

VSS

V13

VSS

V16

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V18

VSS

V2

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V28

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V31

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V33

VSS

V35

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V37

VSS

V4

VSS

V5

VSS

V7

VSS

V8

VSS

V9

VSS

W10

VSS

W11

VSS

W14

VSS

W15

VSS

W17

VSS

W19

VSS

W2

VSS

W21

VSS

W23

VSS

W26

VSS

W27

VSS

W29

VSS

W3

VSS

W30

VSS

W32

VSS

W34

VSS

W36

VSS

W38

VSS

W5

VSS

W7

VSS

Y1

VSS

Y12

VSS

Y13

VSS

Y15

VSS

Y17

VSS

Y19

VSS

Y21

VSS

Y23

VSS

Y25

VSS

Y28

VSS

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Y35

VSS

Y37

VSS

Y5

VSS

Y6

VSS

Y8

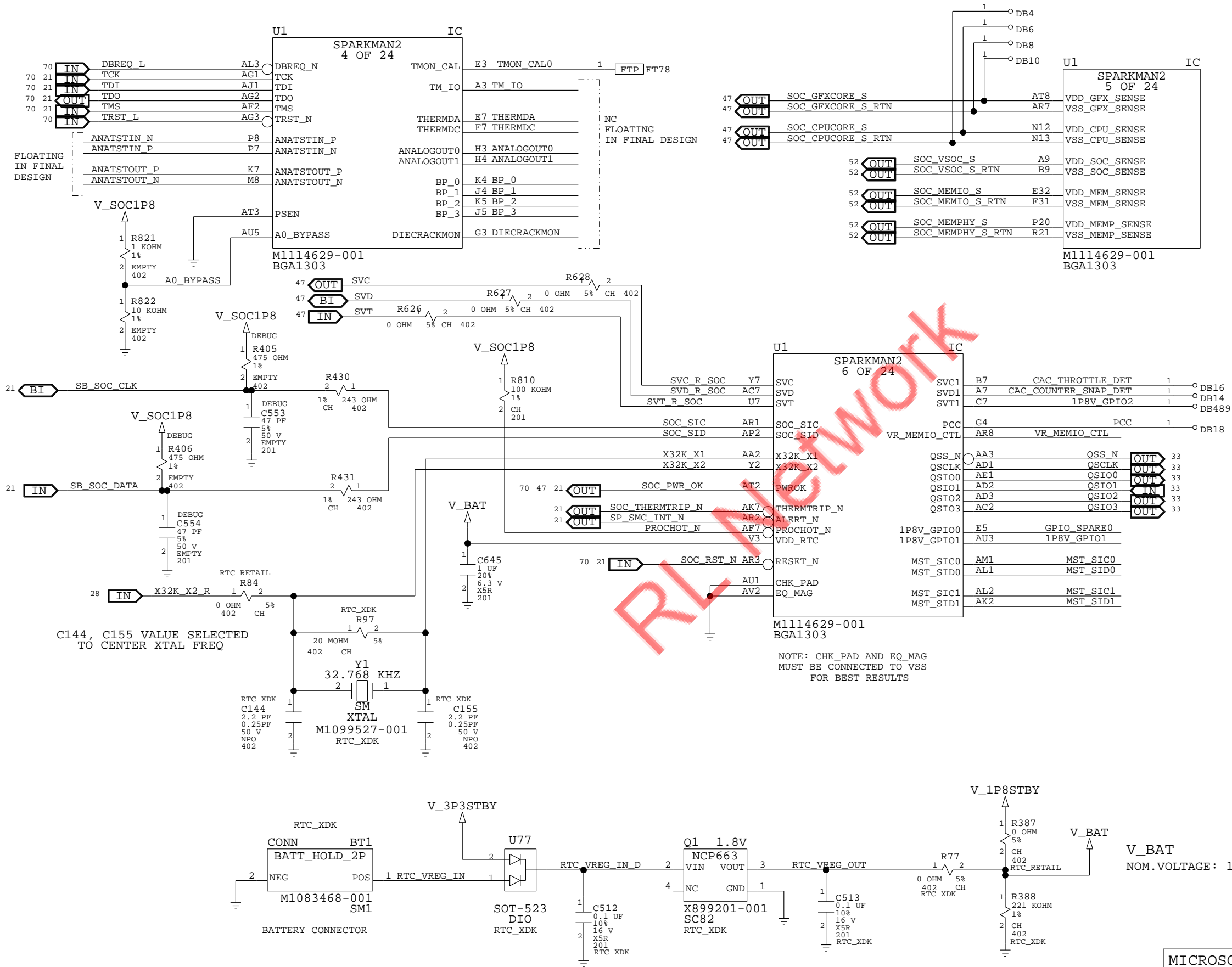
VSS

Y9

M1114629-001
BGA1303

MICROSOFT CONFIDENTIAL	PROJECT NAME Stockton	PAGE 7/76	CSA PAGE 7/76	FAB C	VER 0.12
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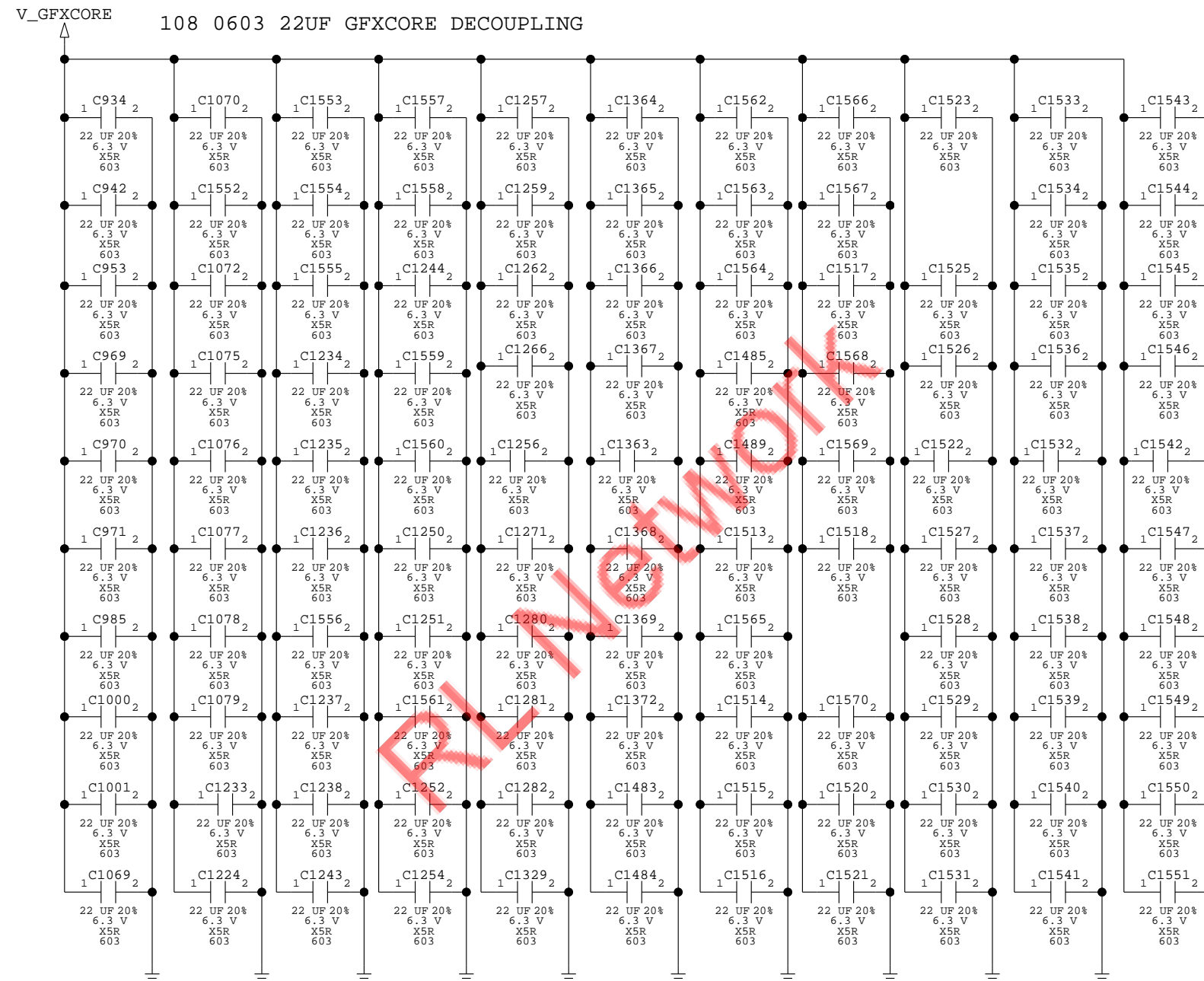
SOC: DEBUG, SB SIGNALS, V_BAT, VOLTAGE SENSE

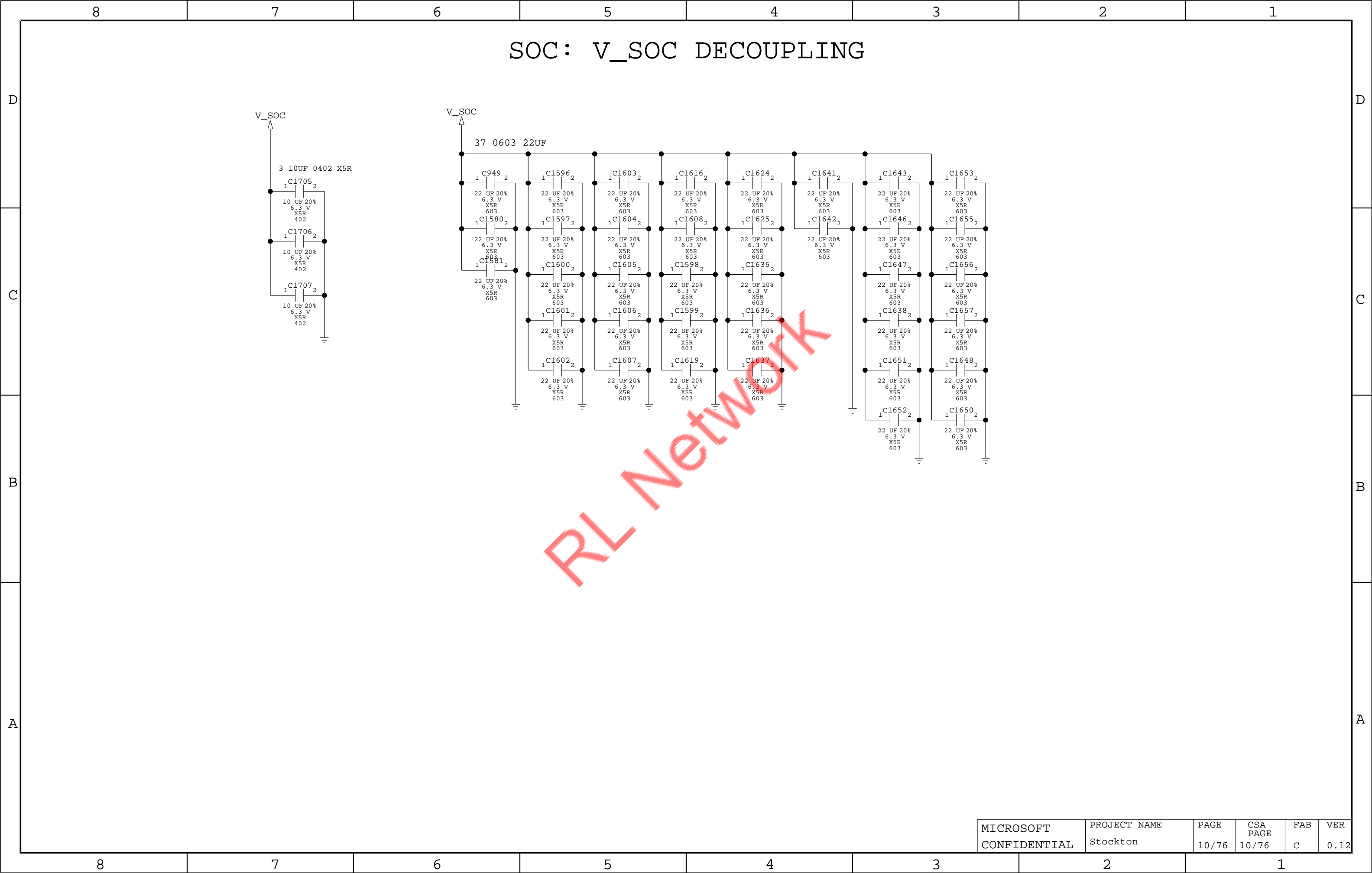


STUFF R388 IF SOC IS NOT STUFFED

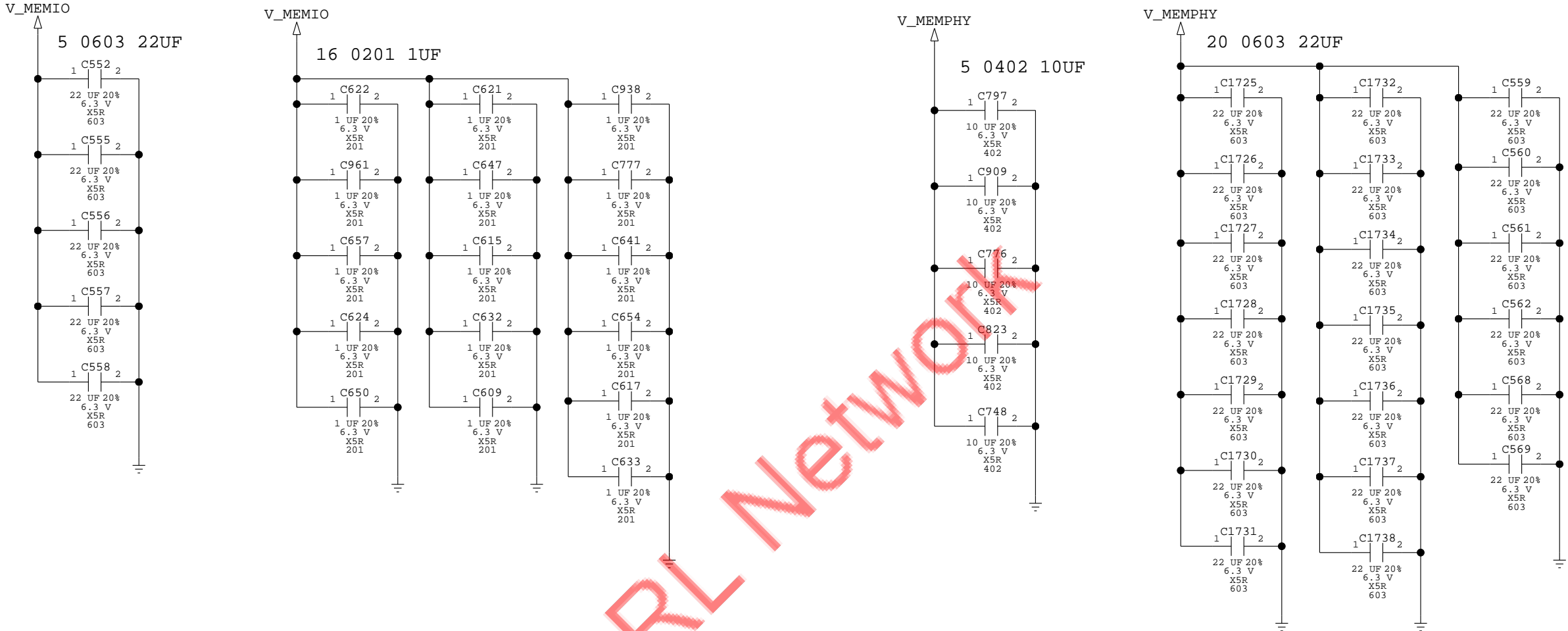
MICROSOFT	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
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SOC: V_GFXCORE DECOUPLING

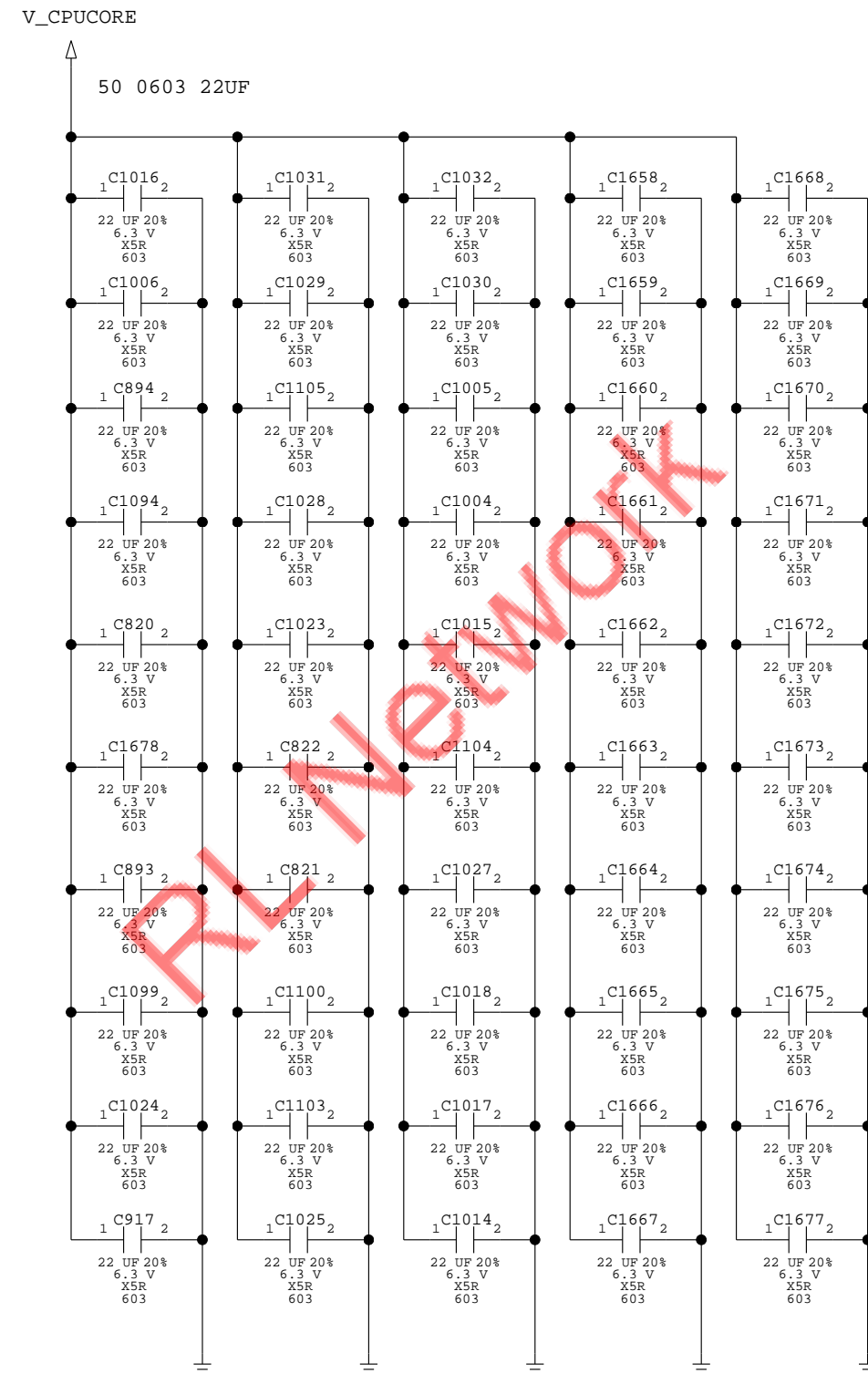




SOC: V_MEMIO/V_MEMPHY DECOUPLING



SOC: V_CPUCORE DECOUPLING

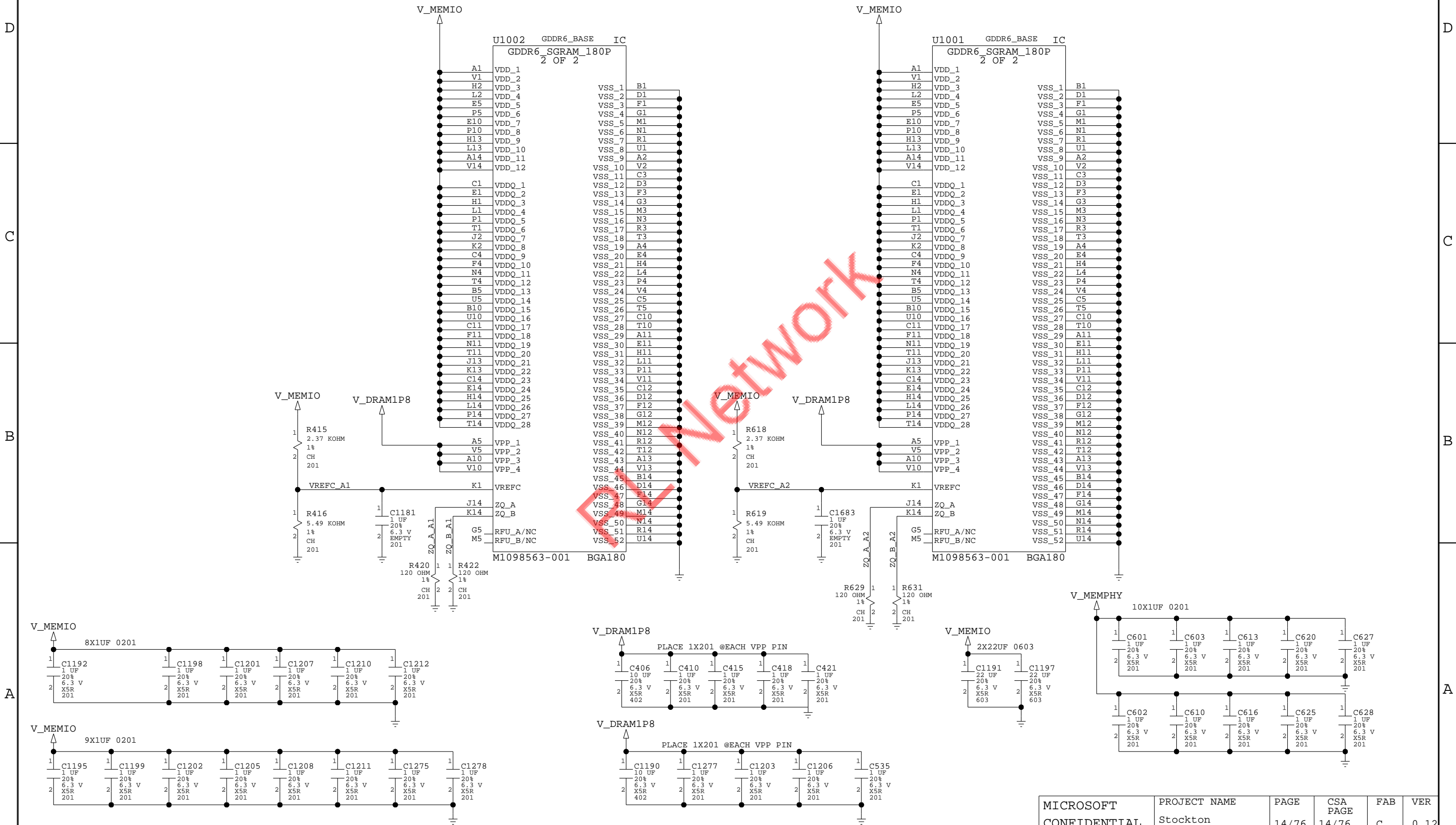


8	7	6	5	4	3	2	1
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A

8	7	6	5	4	3	2	1
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MEMORY: PWR/VSS & DECAP, A



SOC & Memory: CHB/PHY1

U1 SPARKMAN2 9 OF 24 IC

U1 SPARKMAN2 10 OF 24 IC

U1005 GDDR6_BASE IC

GDDR6_SGRAM_180P 1 OF 2

M1114629-001 BGA1303

M1114629-001 BGA1303

M1098563-001 BGA180

GLITCH PROTECTION CIRCUIT FOR RESET

MICROSOFT CONFIDENTIAL

PROJECT NAME Stockton

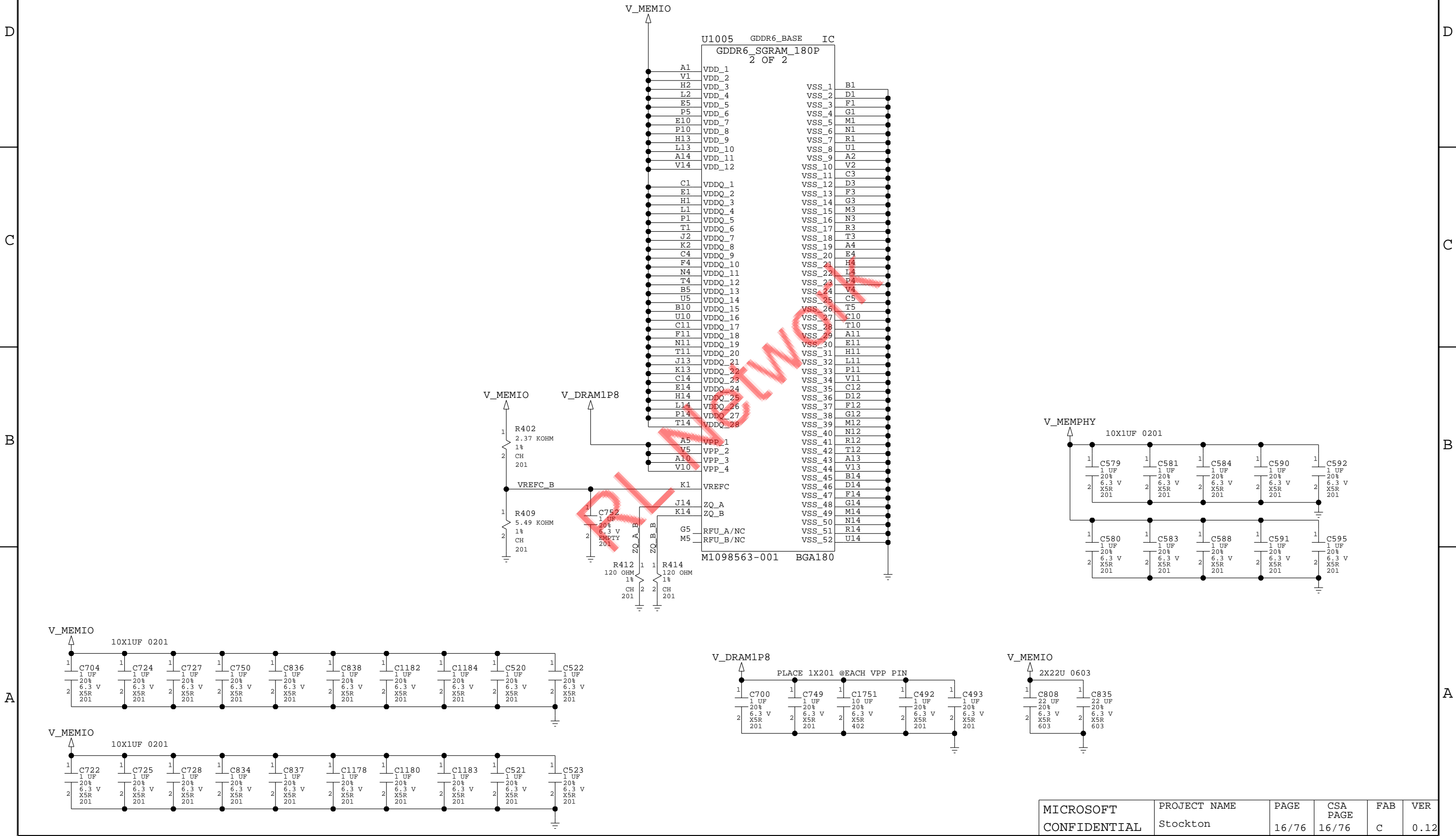
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MEMORY: PWR/VSS & DECAP, B



SOC & Memory: CHC/PHY2

U1 SPARKMAN2 11 OF 24

U1006 GDDR6_BASE IC GDDR6_SGRAM_180P 1 OF 2

U1 SPARKMAN2 12 OF 24

U1098563-001 BGA180

GLITCH PROTECTION CIRCUIT FOR RESET

MICROSOFT CONFIDENTIAL

PROJECT NAME Stockton

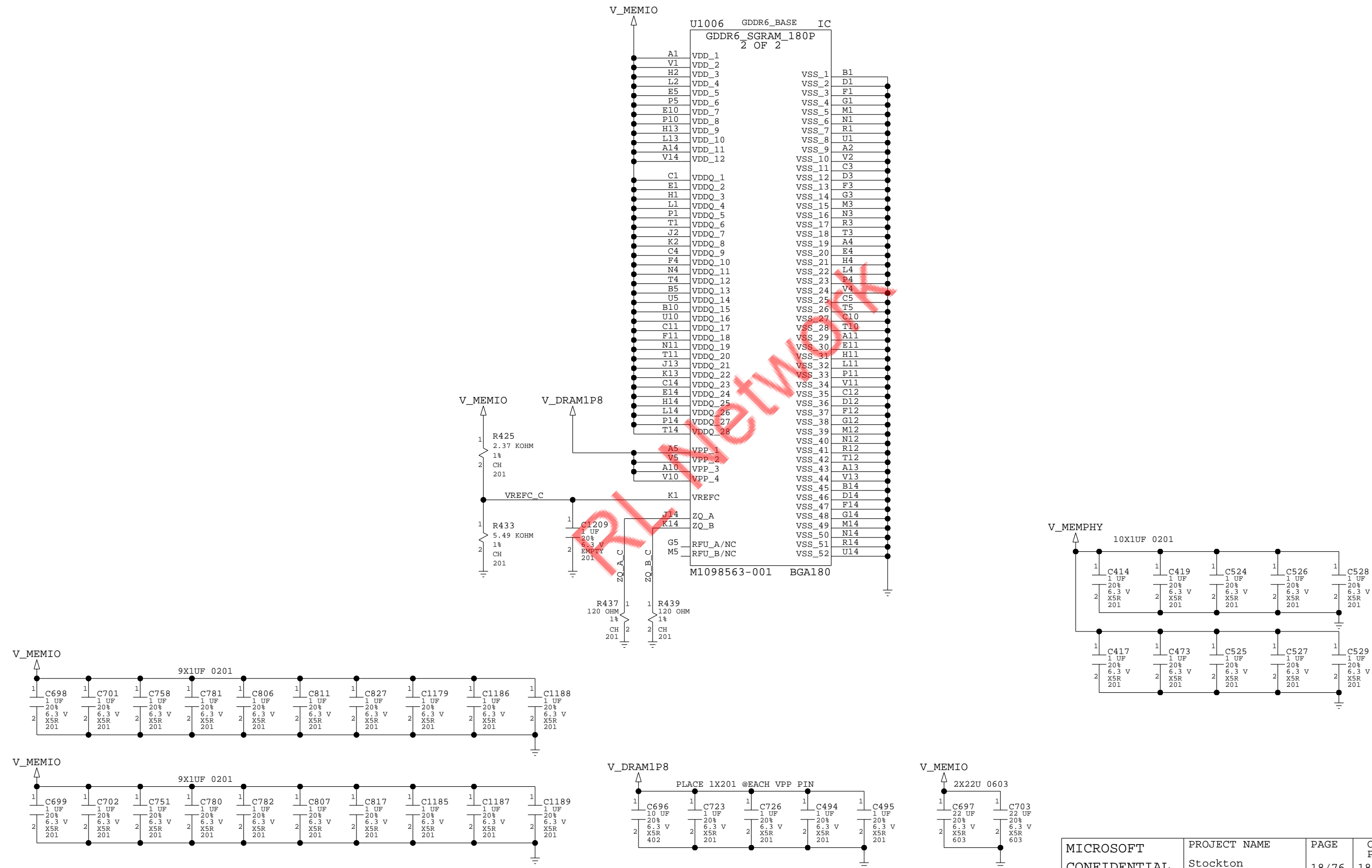
PAGE 17/76

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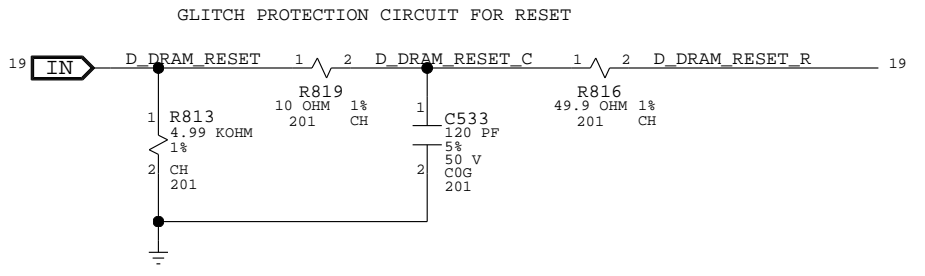
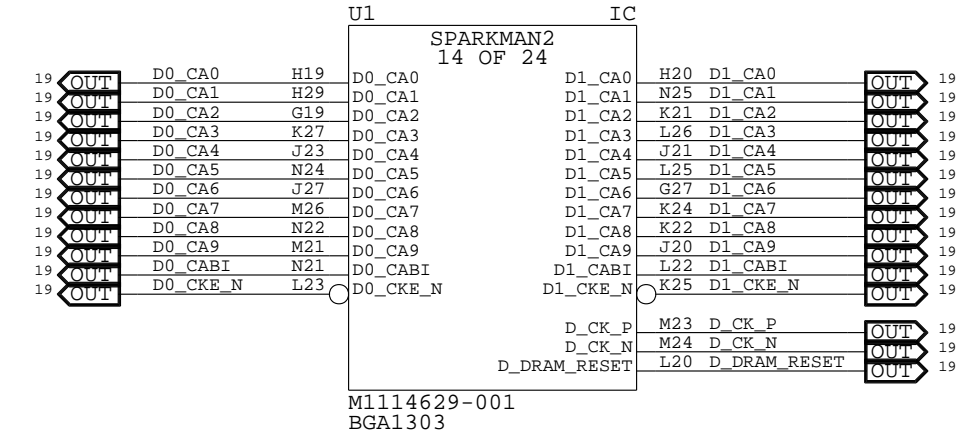
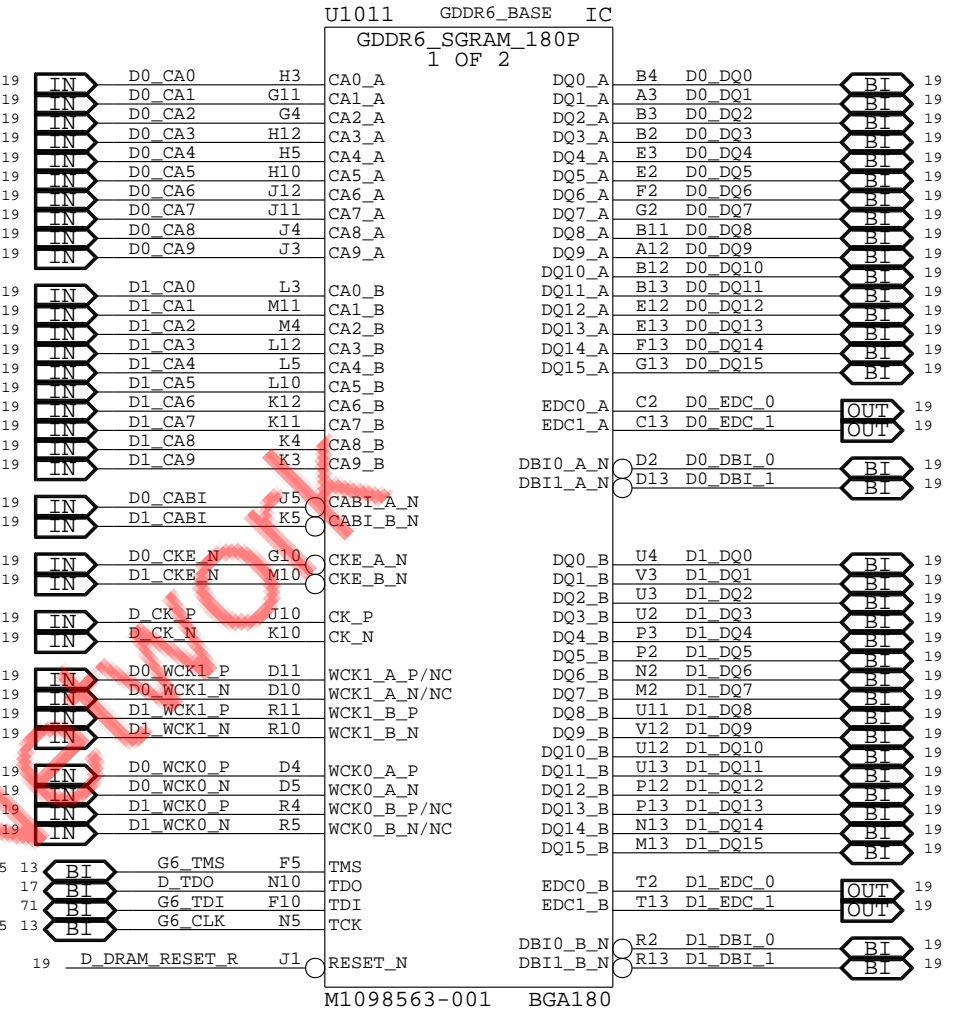
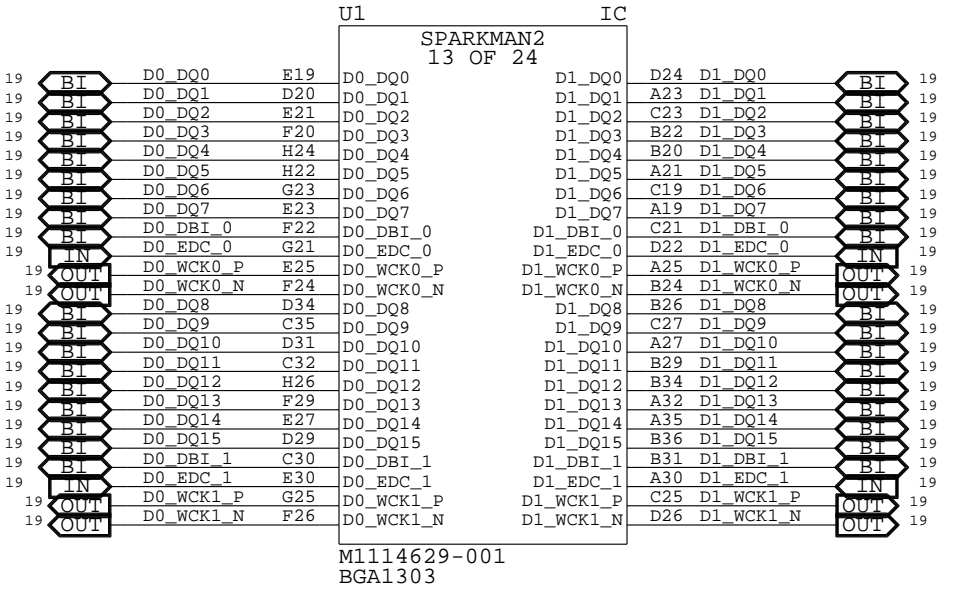
FAB C

VER 0.12

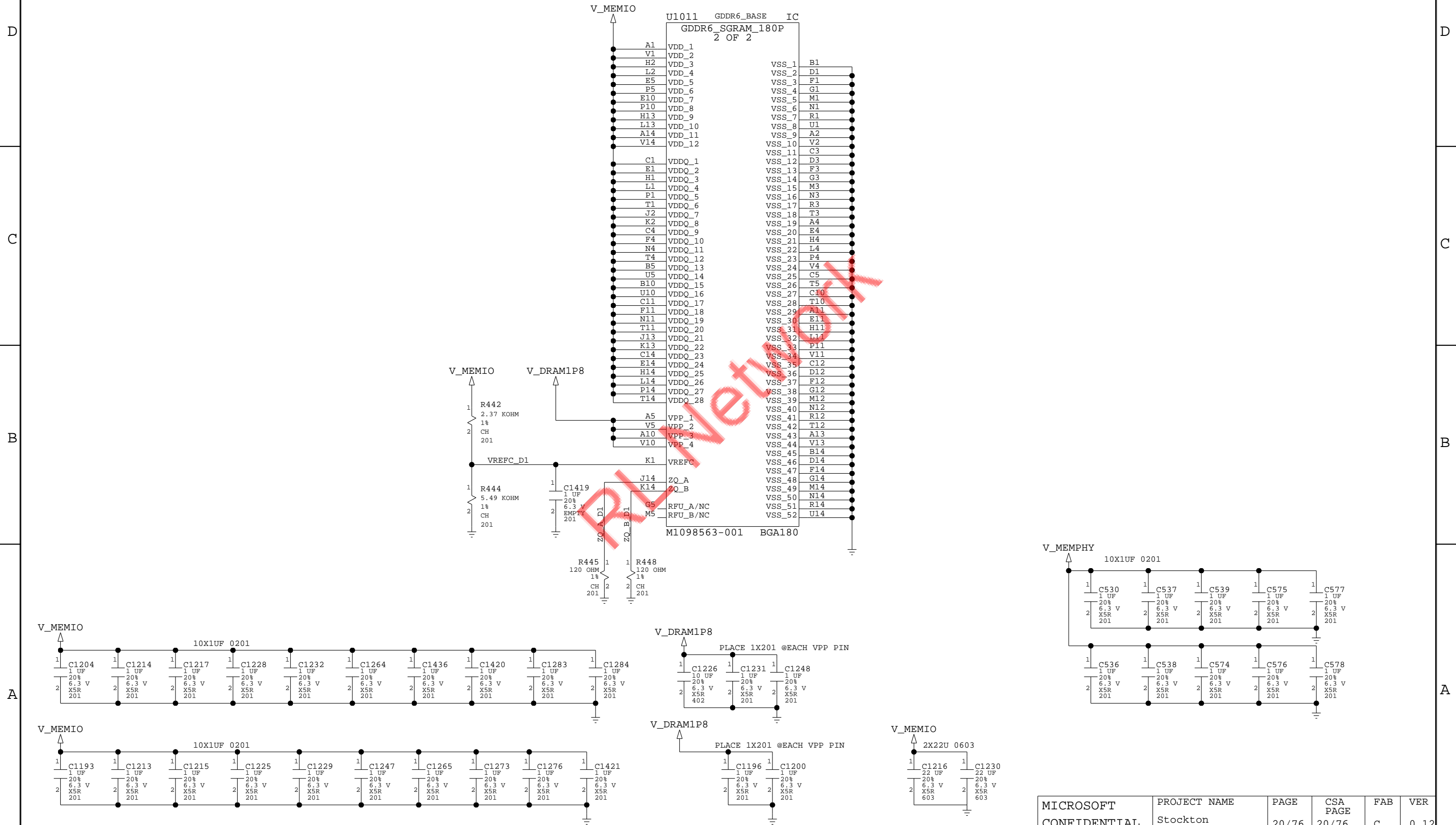
MEMORY: PWR/VSS & DECAP, C

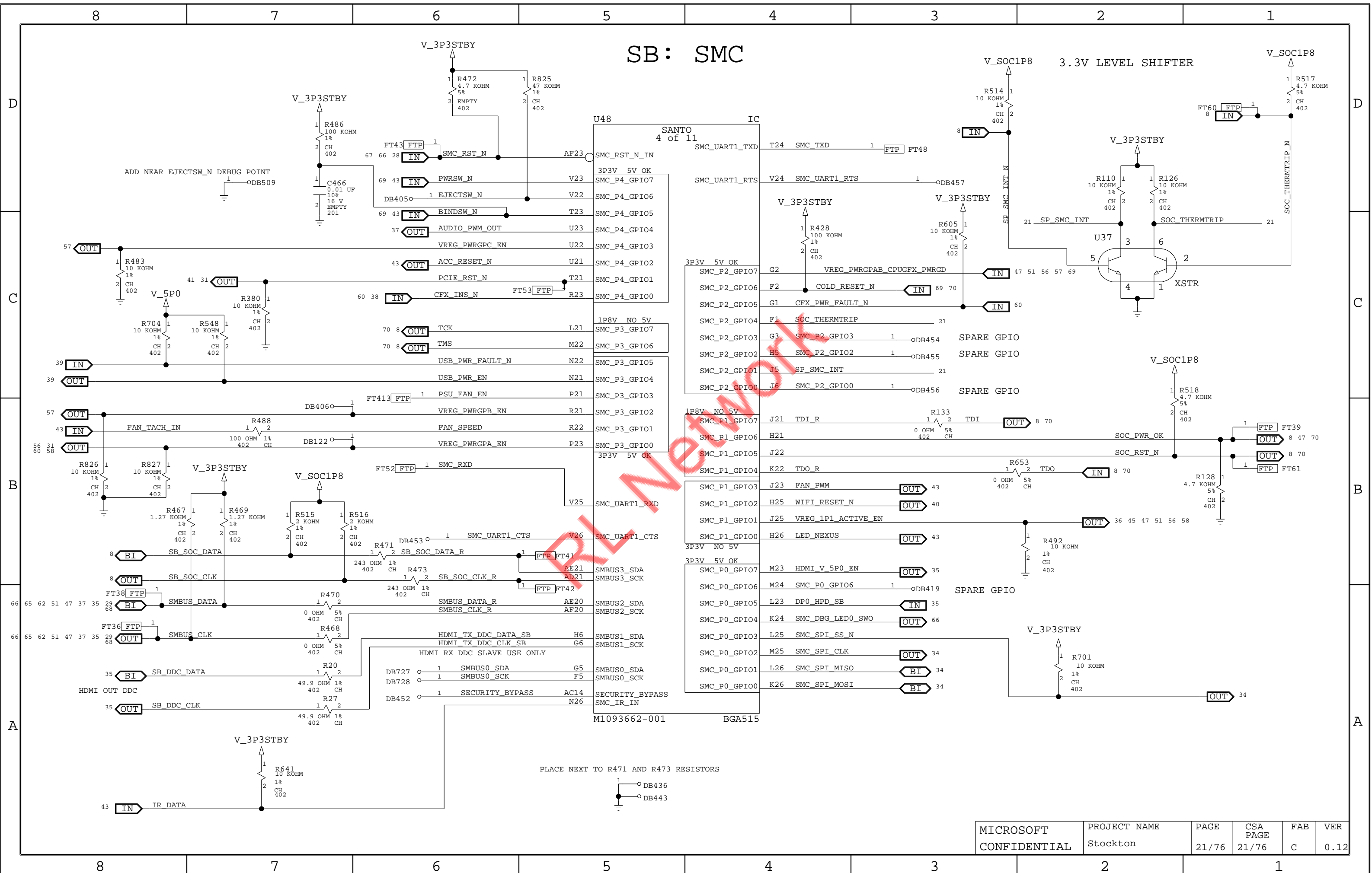


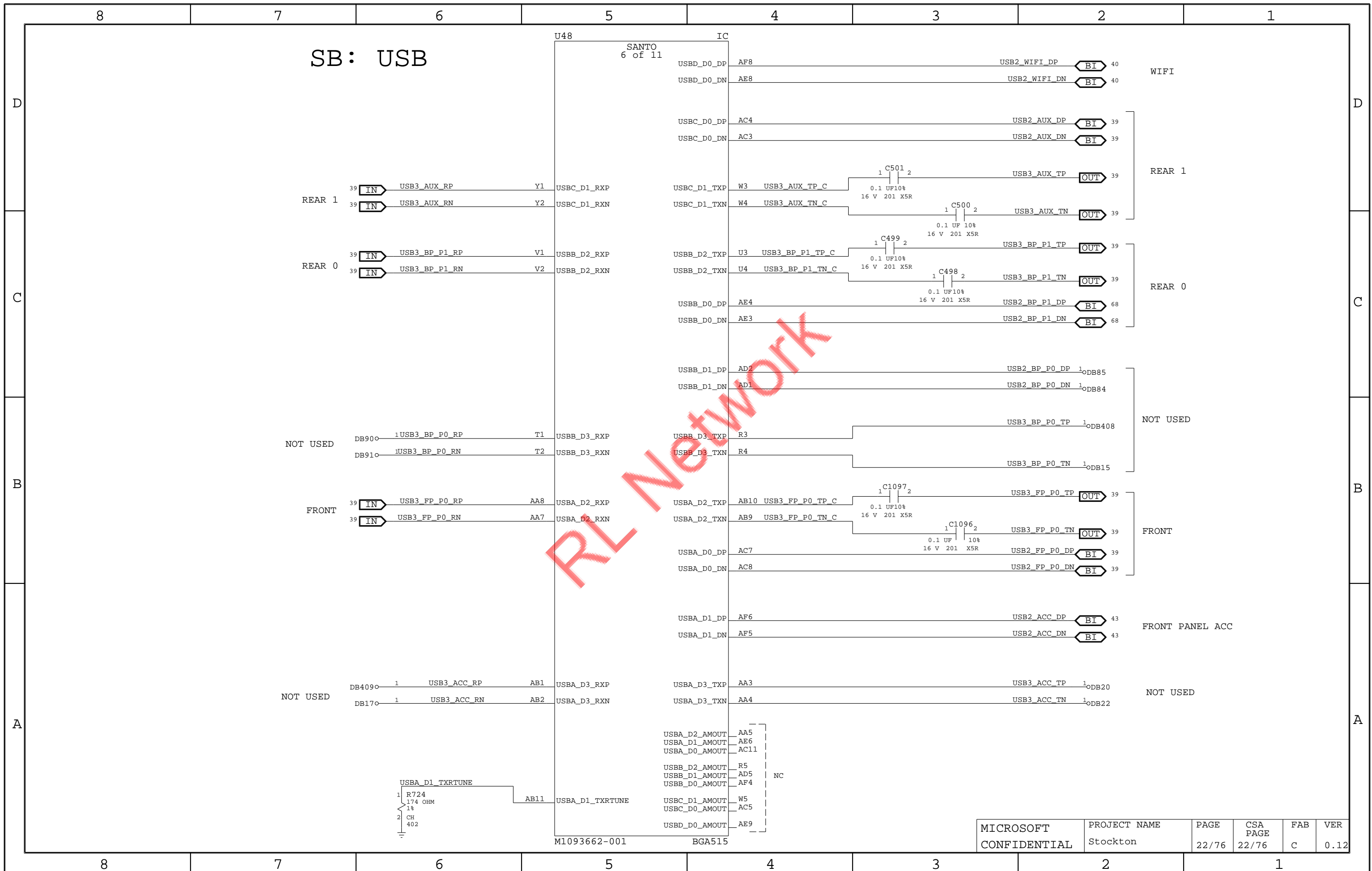
SOC & Memory: CHD/PHY3



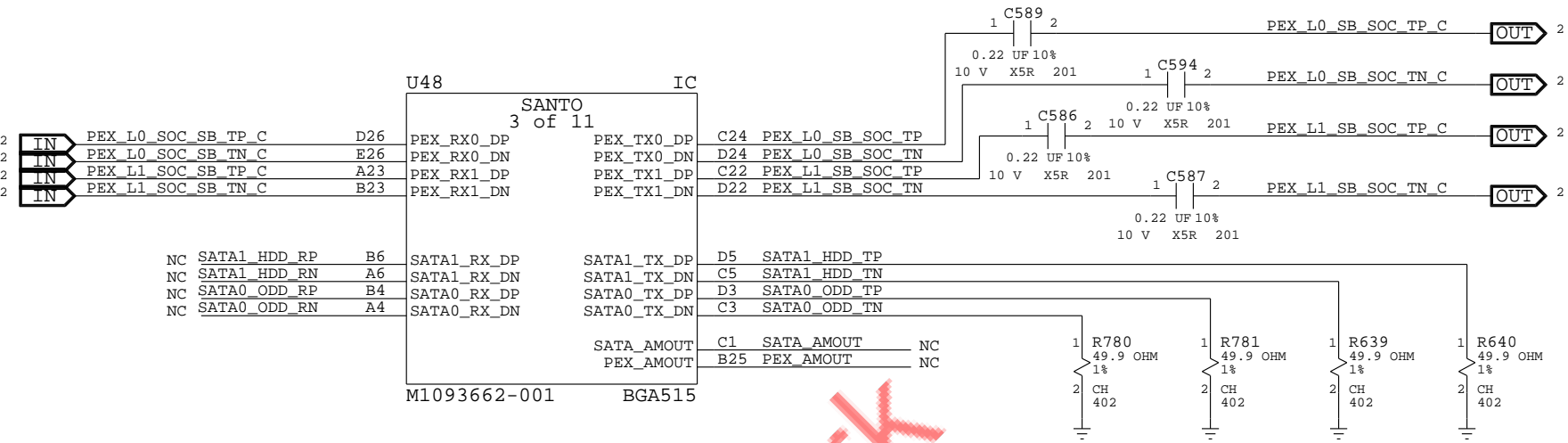
MEMORY: PWR/VSS & DECAP, D



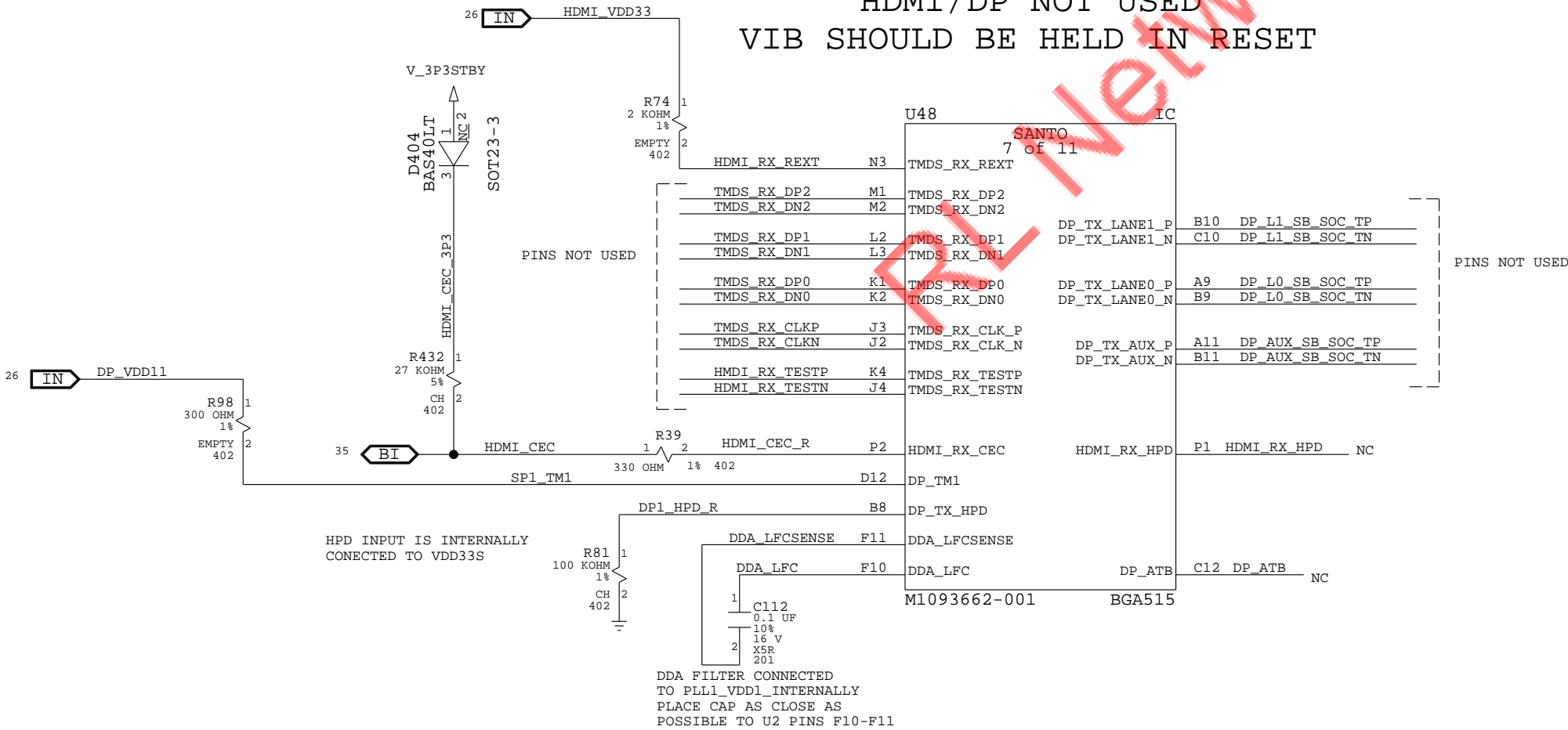




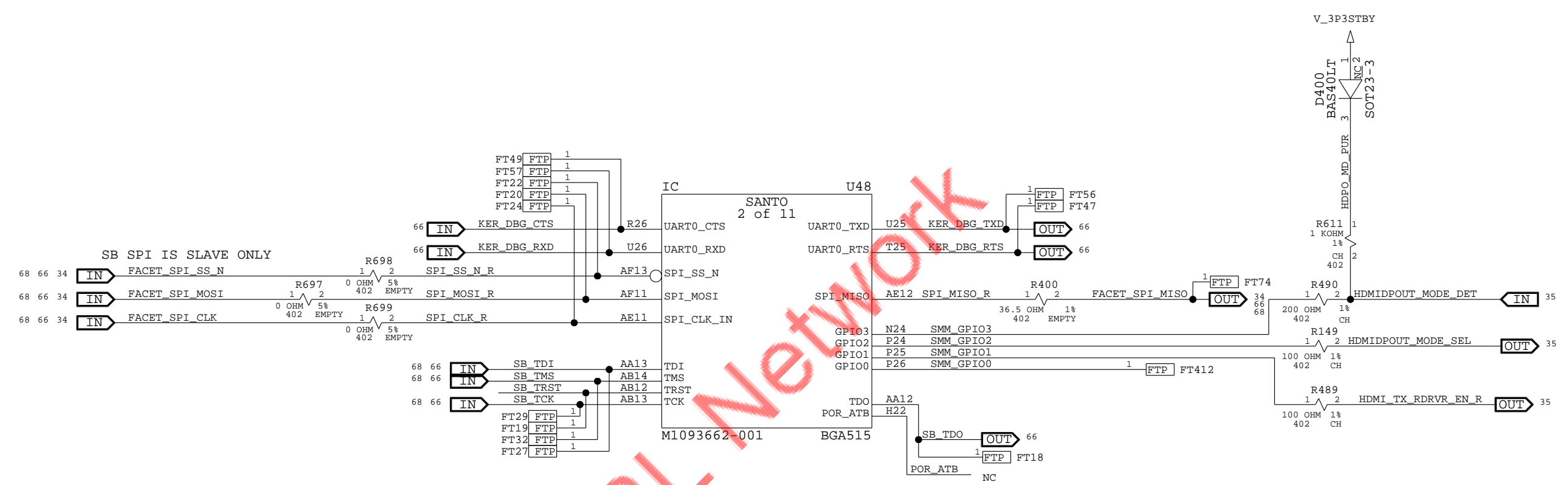
SB: PCIE, SATA, VIDEO

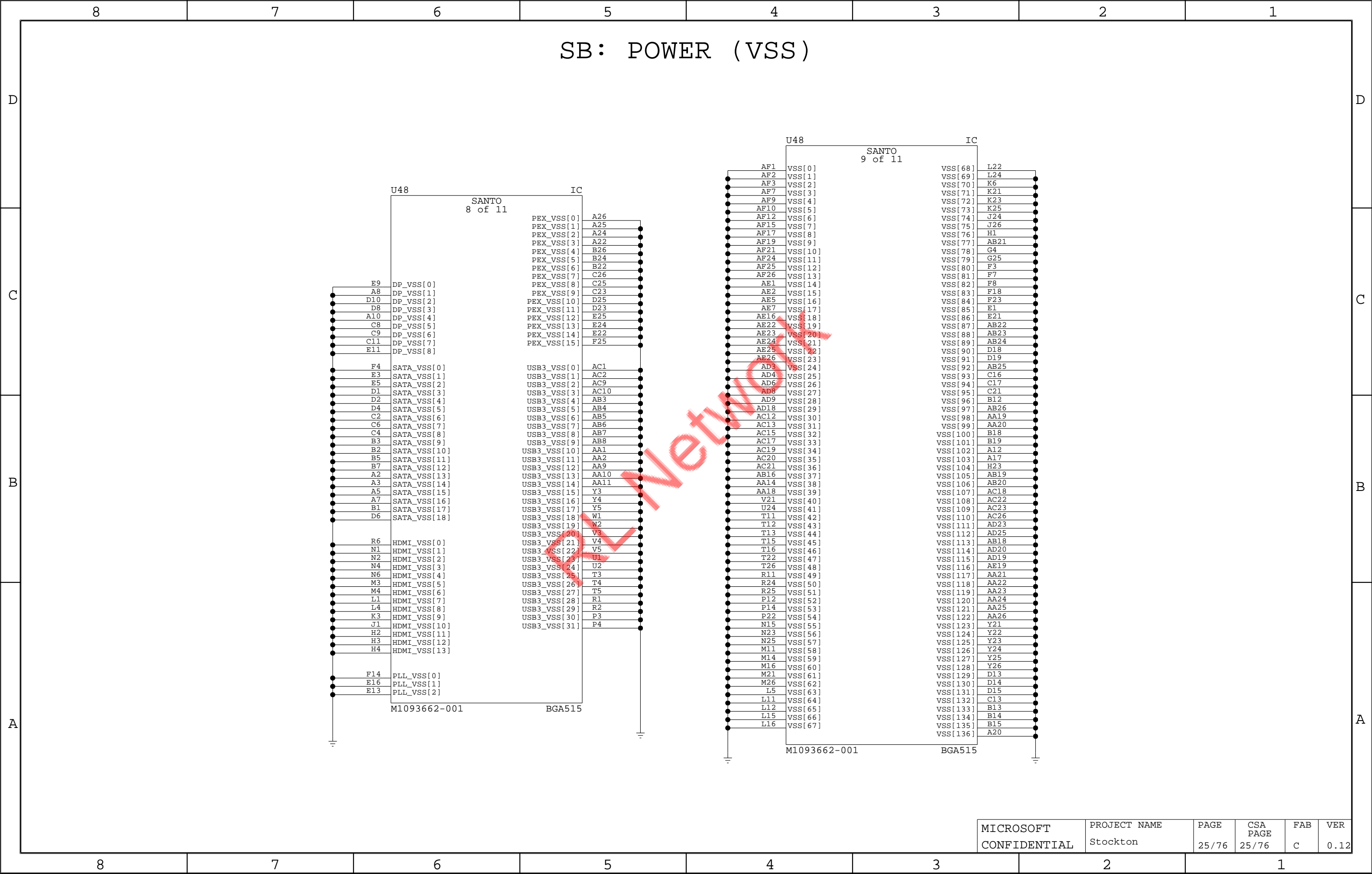


HDMI/DP NOT USED
VIB SHOULD BE HELD IN RESET



SB: SMM UART, SPI, JTAG, GPIO





SB: POWER

POWER REMOVED FROM AUX AND HDMI

IC

OUT 23

V_3P3

V_SB1P1

V_SB1P1

V_SB1P1

V_SB1P1

V_SB1P1

V_SB1P1

POWER REMOVED FROM DP

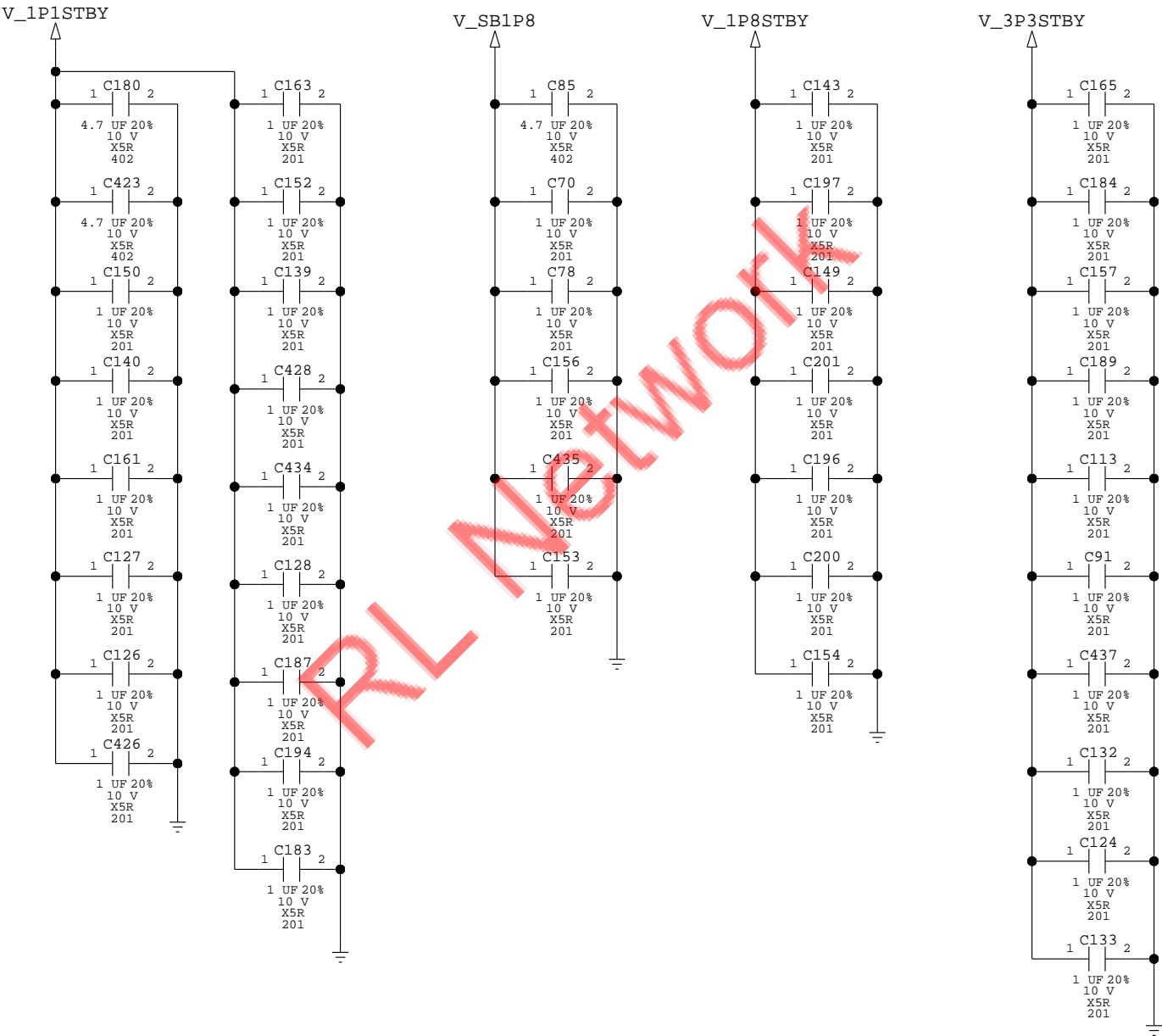
OUT 23

V_SB1P1

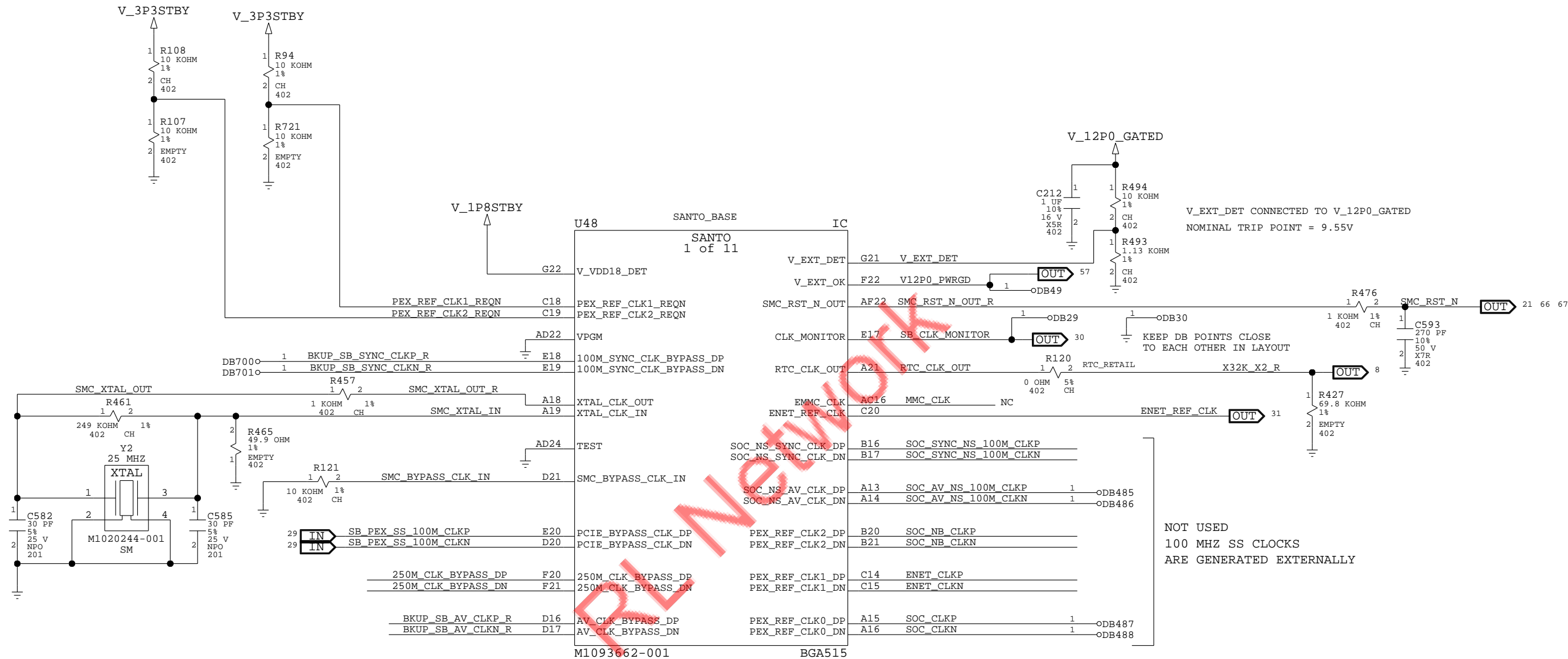
MICROSOFT	PROJECT NAME	PAGE	CSA	FAB	VER
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SB: DECOUPLING

NOTE: ALL V_SB1P1 DECOUPLING
IS SHOWN ON POWER PAGE 49



SB: CLOCKS, STRAPPING, POR



MXXXXXXX-001	MATL	REF DES	DESCR.	BOM PROPERTY
M1093668-001	IC	U48	IC,SANTO SB,BGA515	SANTO_RETAIL
M1093662-001	IC	U48	IC,SANTO SB,BGA515	SANTO_DEV
M1093668-001	EMPTY	U48	IC,SANTO SB,BGA515	SANTO_EMPTY

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CLOCK: PCIE 100MHZ SS

9FGL0651 SMBUS ADDRESS
1101 010 R/W HEX
WRITE 1101 010 0 0XD4
READ 1101 010 1 0XD5

POWER SUBJECT TO REVIEW

85 OHM DIFF OUTPUTS

R166 = 1K TO ACCOUNT FOR ~60KOHM COMBINED INPUT IMPEDANCE OF CLOCK GENS

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I2C BUFFER PREVENTS LEAKAGE PATH FROM SMBUS PULLUPS TO V_3P3_GATED THROUGH CLOCK GENERATORS

EN: 450K INTERNAL PU TO VCCA
V_3P3_SS_CLK HAS 10K PD TO GND

PLACE NEXT TO I2C ISOLATION RESISTORS

PLACE NEXT TO I2C ISOLATION RESISTORS

D

C

B

A

D

C

B

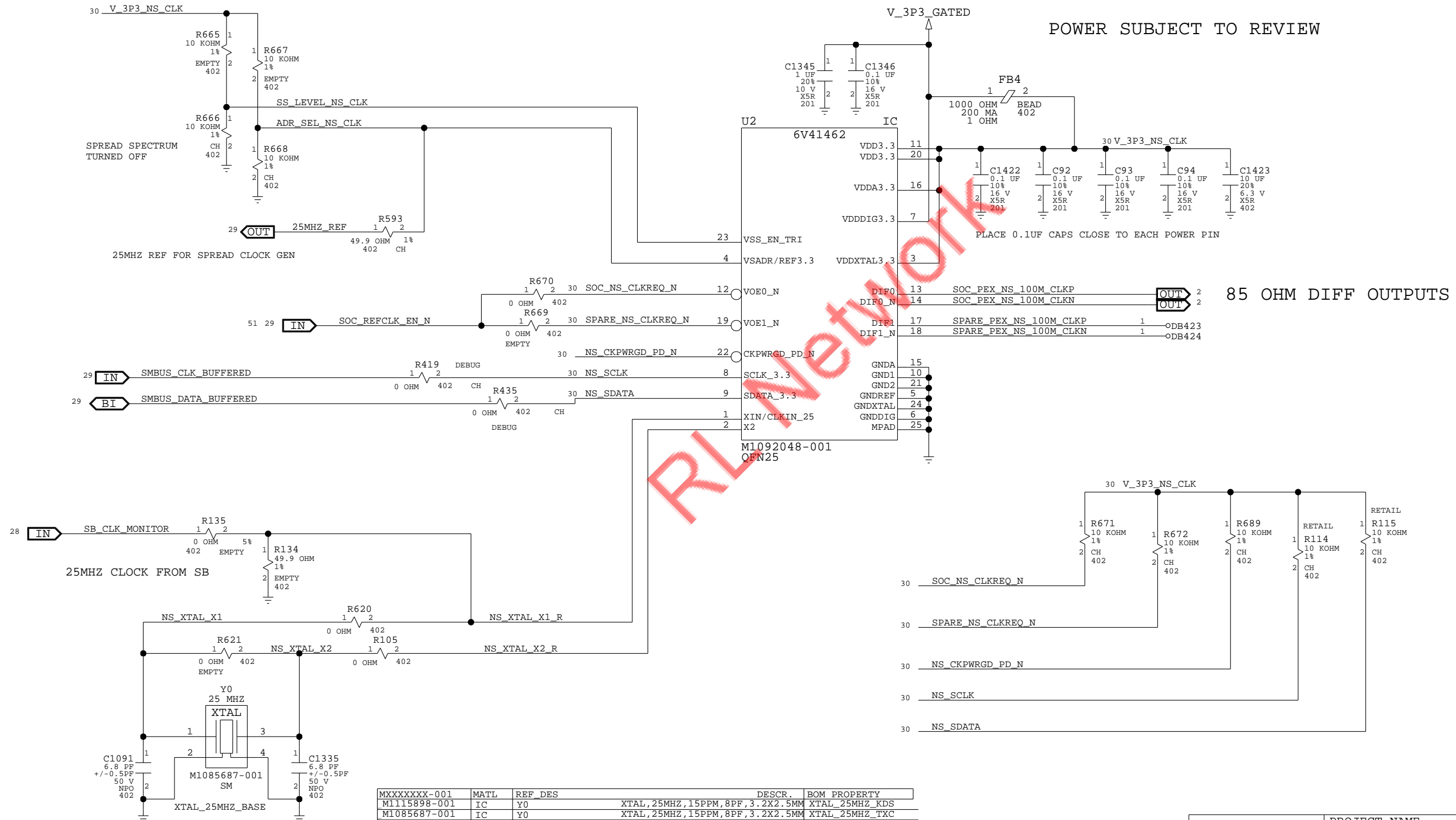
A

CLOCK: PCIE 100MHZ NS

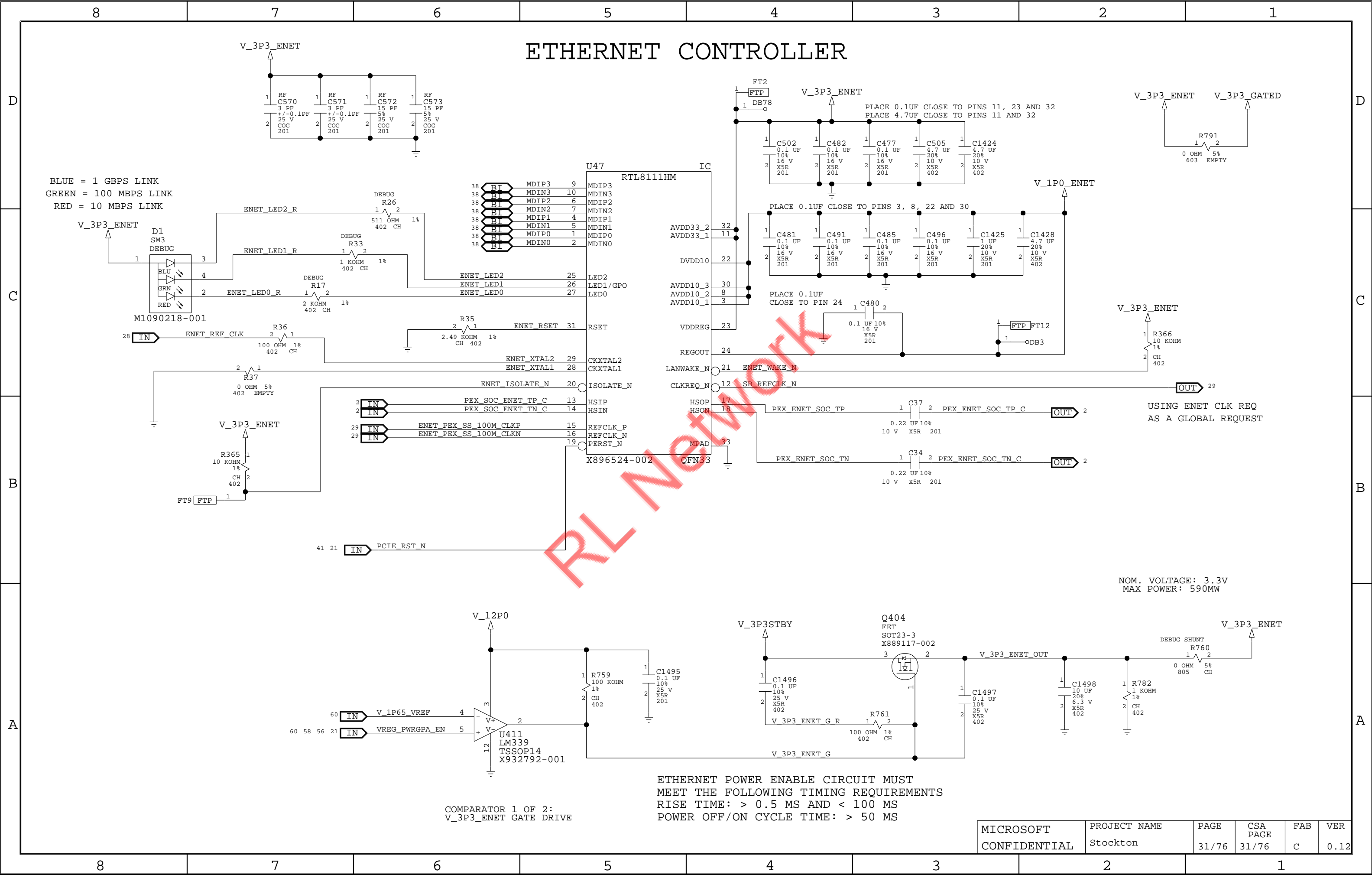
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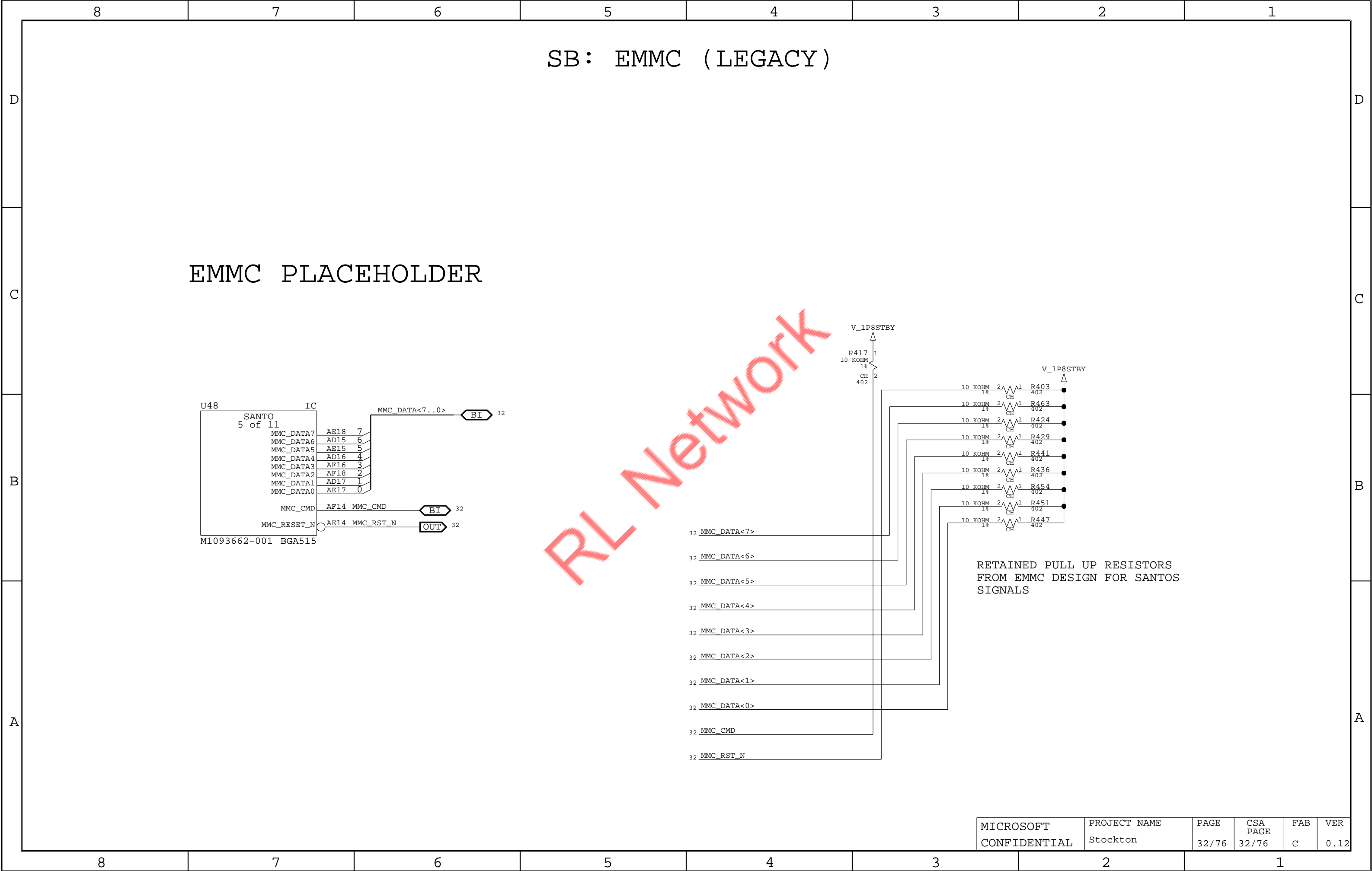
9FGL04 SMBUS ADDRESS
      1101 000  R/W HEX
WRITE 1101 000   0 0XD0
READ  1101 000   1 0XD1

```



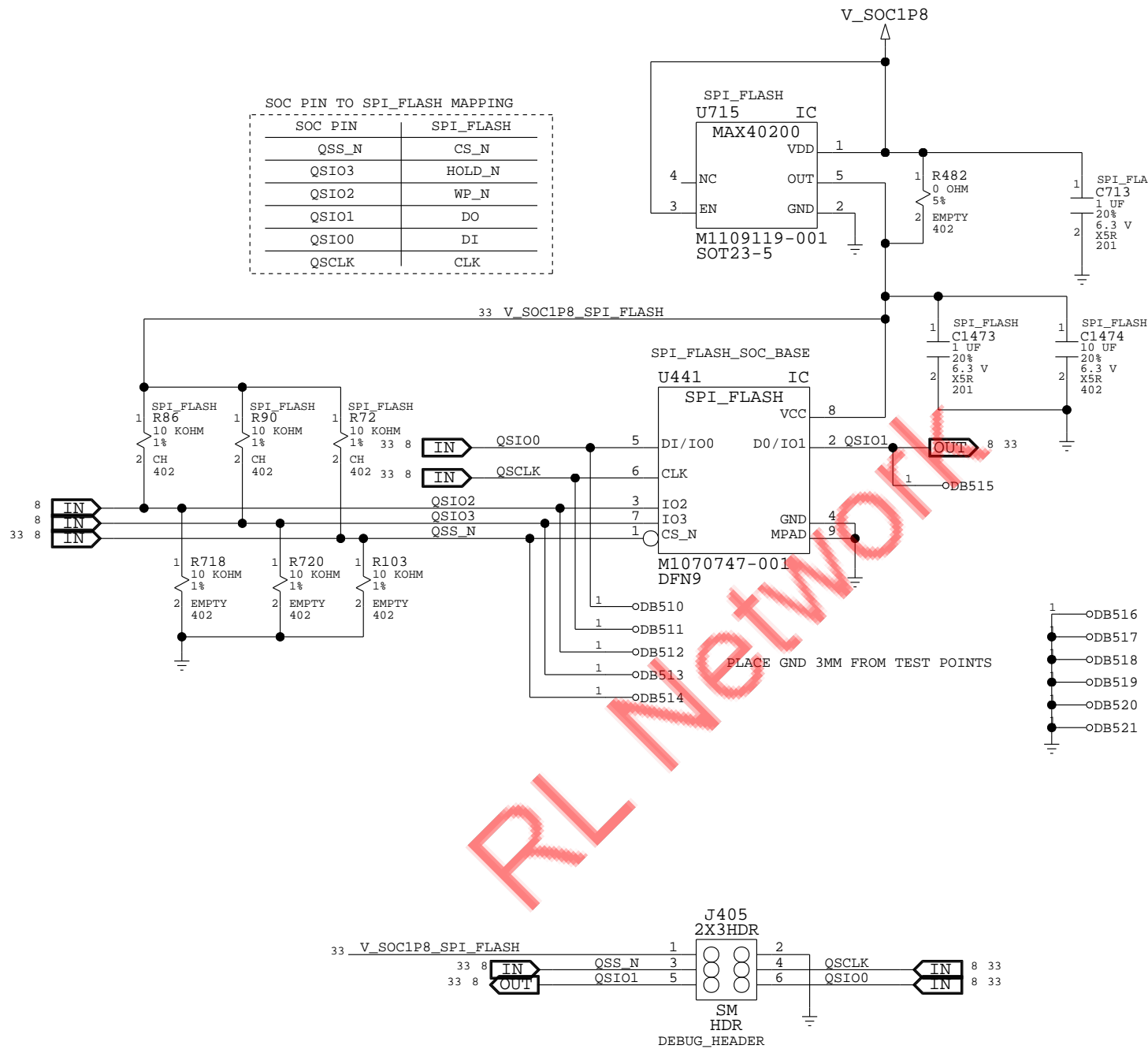
MXXXXXXX-001	MATL	REF	DES	DESCR.	BOM PROPERTY
M115898-001	IC	Y0		XTAL, 25MHZ, 15PPM, 8PF, 3.2X2.5MM	XTAL_25MHZ_KDS
M1085687-001	IC	Y0		XTAL, 25MHZ, 15PPM, 8PF, 3.2X2.5MM	XTAL_25MHZ_NDK
M115904-001	IC	Y0		XTAL, 25MHZ, 15PPM, 8PF, 3.2X2.5MM	XTAL_25MHZ_TXC





MEMORY: SPI FLASH SOC

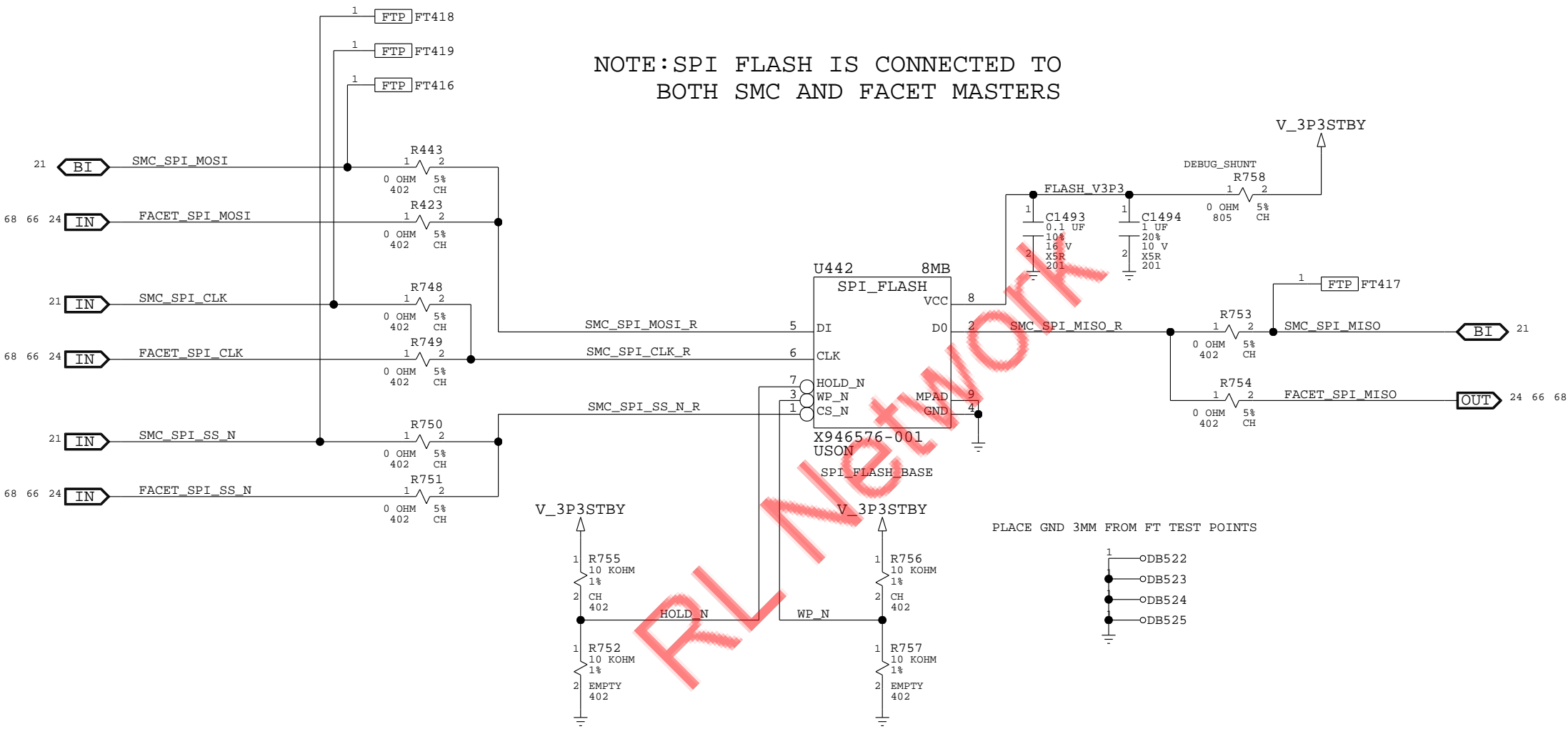
MAX40200 IDEAL DIODE PROVIDES BACKDRIVE PROTECTION FROM DEDIPROG



MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
M1070747-001	IC	U441	FLASH MEMORY,FLASH,256MBIT,SM,WS08, SERIAL,W/DUAL/QUAD SPI	SPI_FLASH_SOC_WINBOND
M1104466-001	IC	U441	FLASH MEMORY,FLASH,256MBIT,SM,8-WS08, SERIAL,MULTI I/O,DTR,1.8V	SPI_FLASH_SOC_MACRONIX

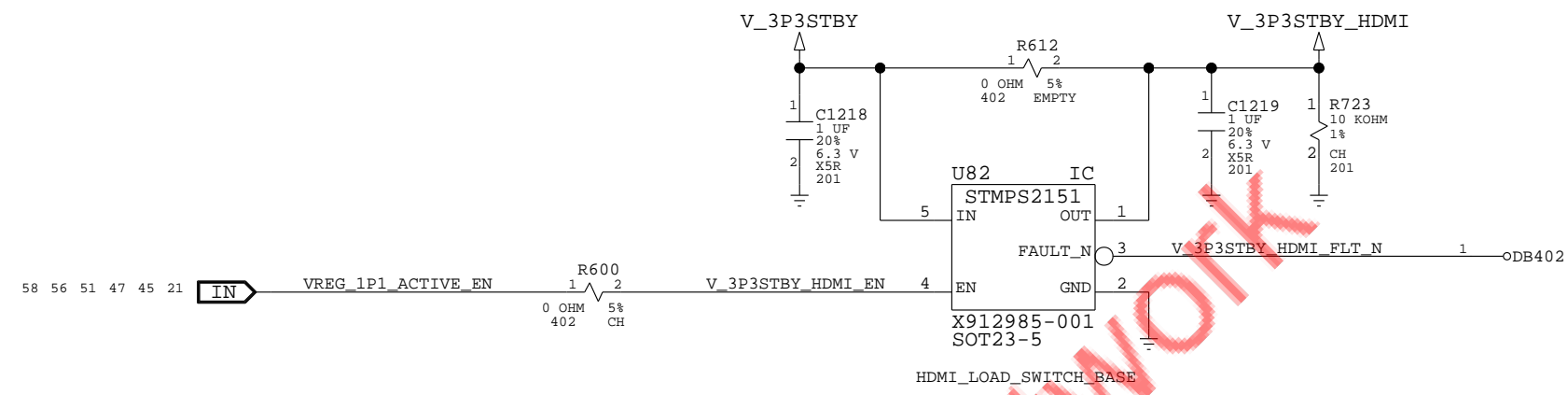
MEMORY: SPI FLASH

NOTE:SPI FLASH IS CONNECTED TO BOTH SMC AND FACET MASTERS



XXXXXXXX-001	MATL	REF DES	DESCR.	BOM PROPERTY
X946576-001	IC	U442	WINBOND,SPI_FLASH,8GBIT,USON	SPI_FLASH_WINBOND
M1090771-001	IC	U442	MACRONIX,SPI_FLASH,8GBIT,USON	SPI_FLASH_MACRONIX

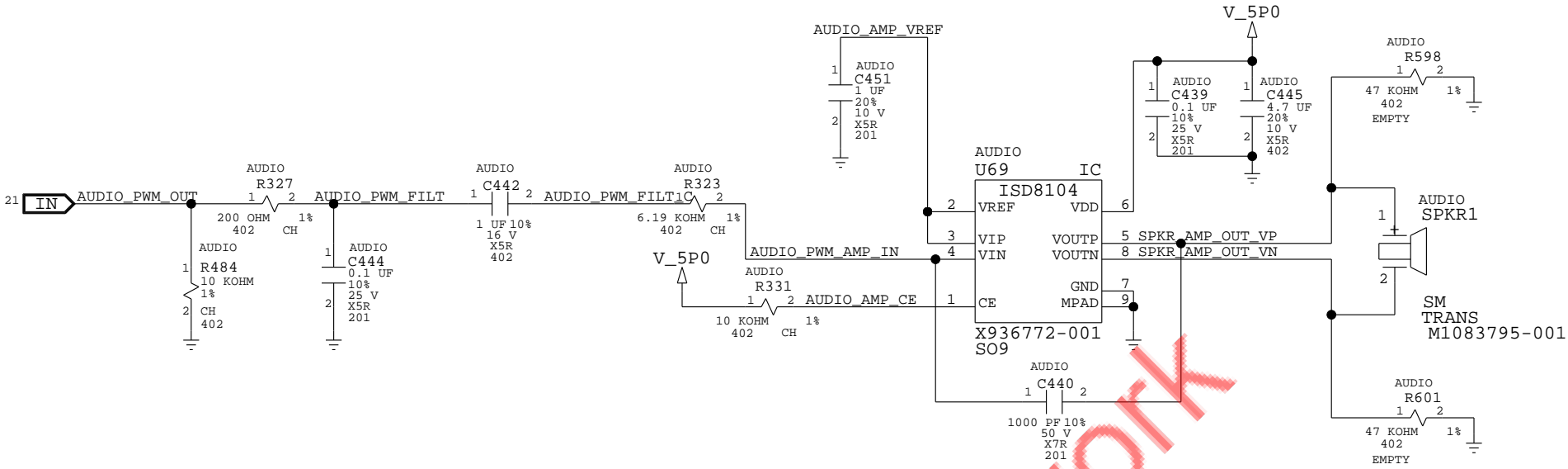
HDMI : LOAD SWITCHES



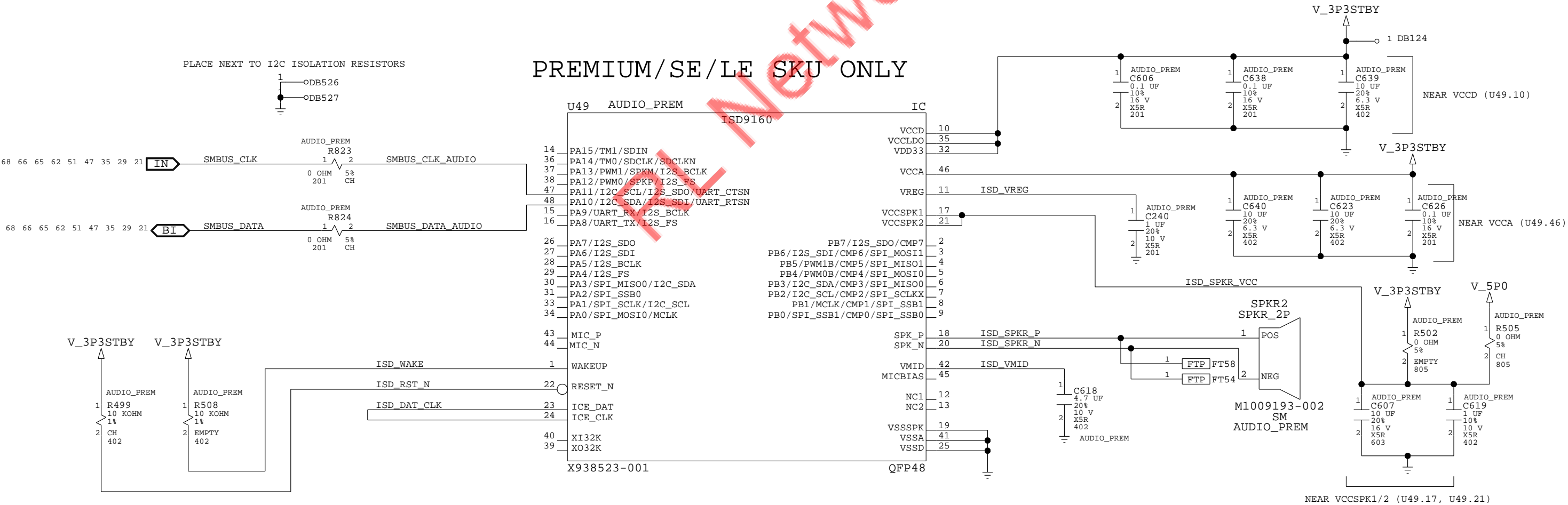
U82 IS MITIGATION FOR HDMI TMDS BACK-DRIVE CURRENT THROUGH Q621M RE-DRIVER

MXXXXXX-001	MATL	REF	DES	DESCR.	BOM PROPERTY
X912985-001	IC	U82	IC,SM,SOT23-5,STMP2151STR,PWR SW,1CH,0.5A	HDMI_LOAD_SWITCH_ST	
X862402-001	IC	U82	IC,SM,SOT23-5,TPS2065DBVR,HI SIDE SW,1.5A	HDMI_LOAD_SWITCH_TI	
X934019-001	IC	U82	IC,SM,SOT23-5,AP2151D,PWR SW,1CH,0.5A,DIODES QUAL	HDMI_LOAD_SWITCH_DIODES	

AUDIO: PREMIUM AND RETAIL



PREMIUM/SE/LE SKU ONLY



ISD9160FIMS05 - REMOVED CAP TOUCH FUNCTIONALITY

CONN: RJ45, SPDIF, CFEXPRESS

MXXXXXXX-001	MATL	REF DES	DESCR.	BOM PROPERTY
M1087814-001	CONN	J13	FOXCONN RJ45 CONNECTOR	CON_RJ45_FOXC
MXXXXXXX-001	CONN	J13	AMPHENOL QUAL RJ45 CONNECTOR	CON_RJ45_AMP

D

D

C

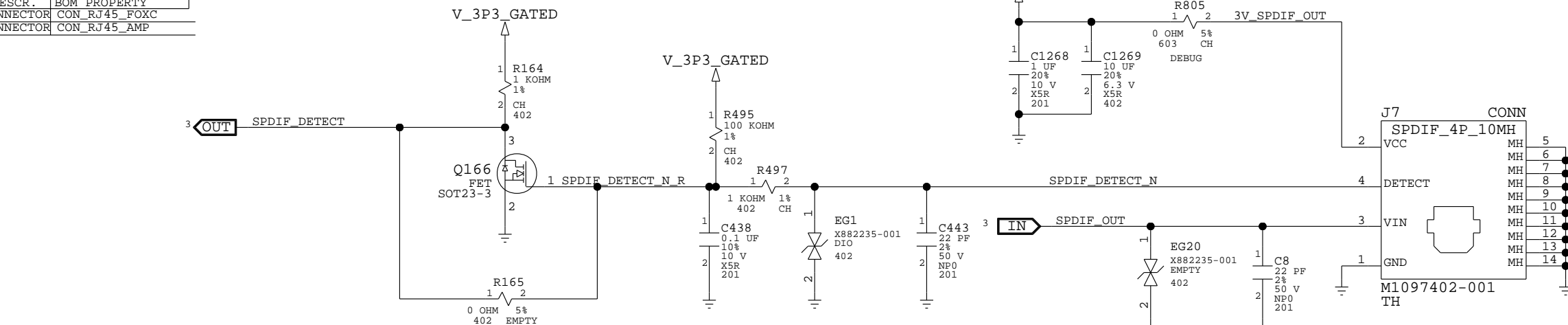
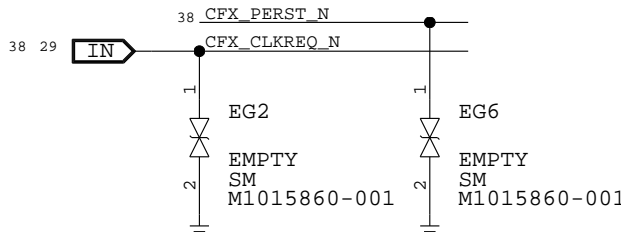
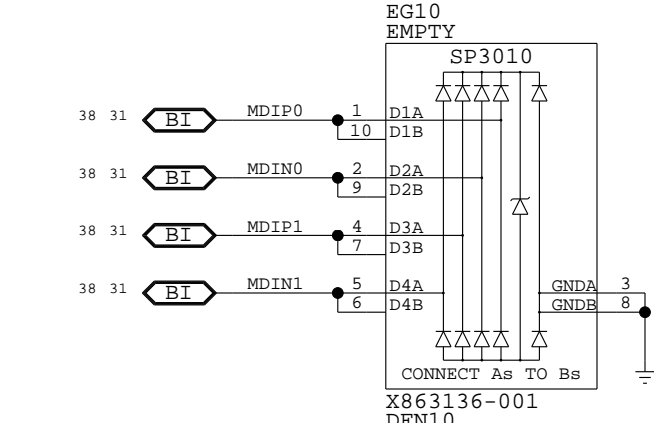
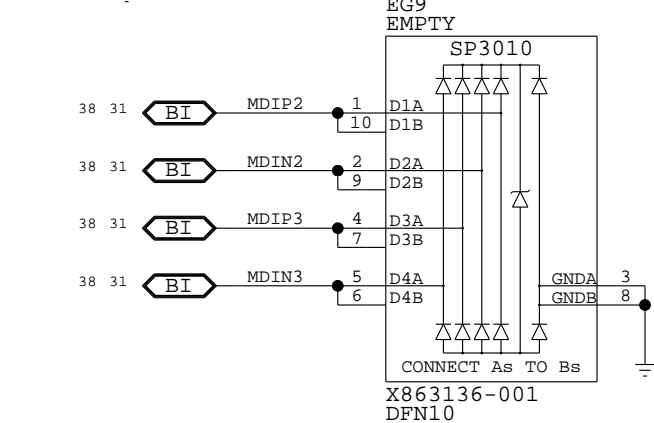
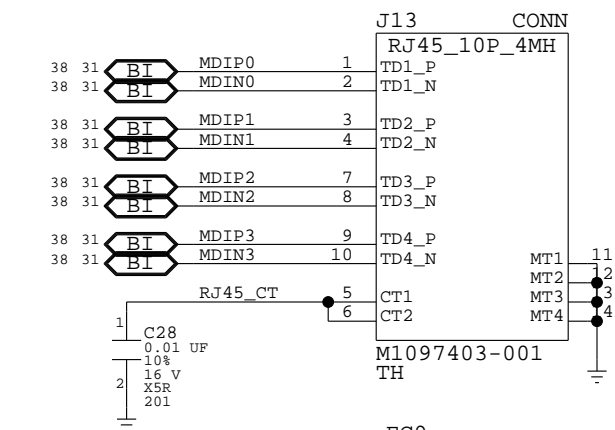
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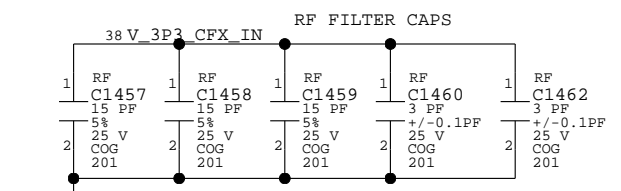
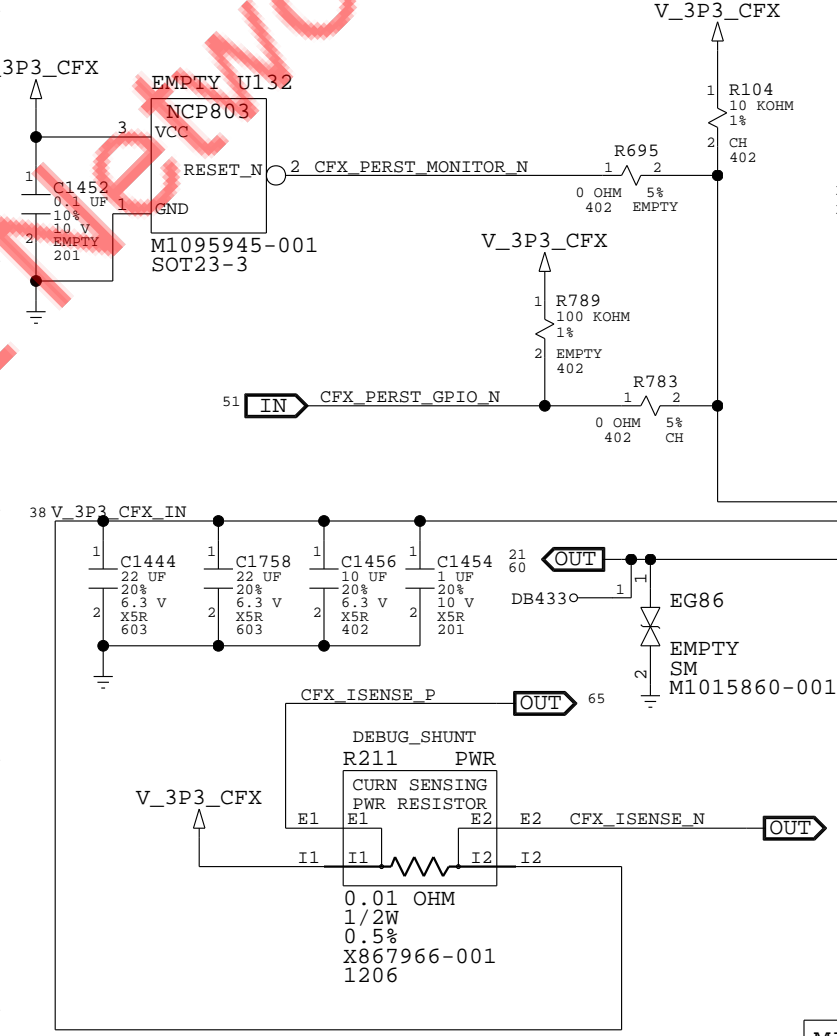
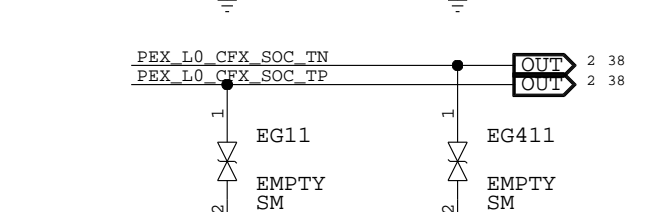
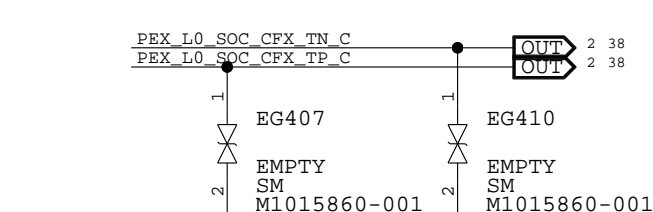
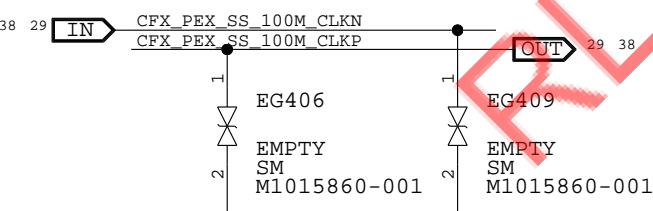
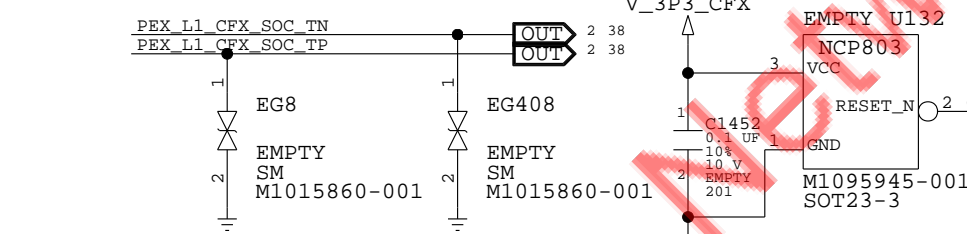
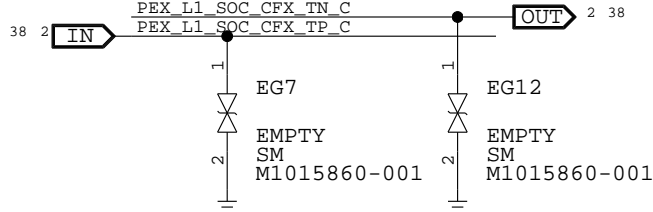
B

A

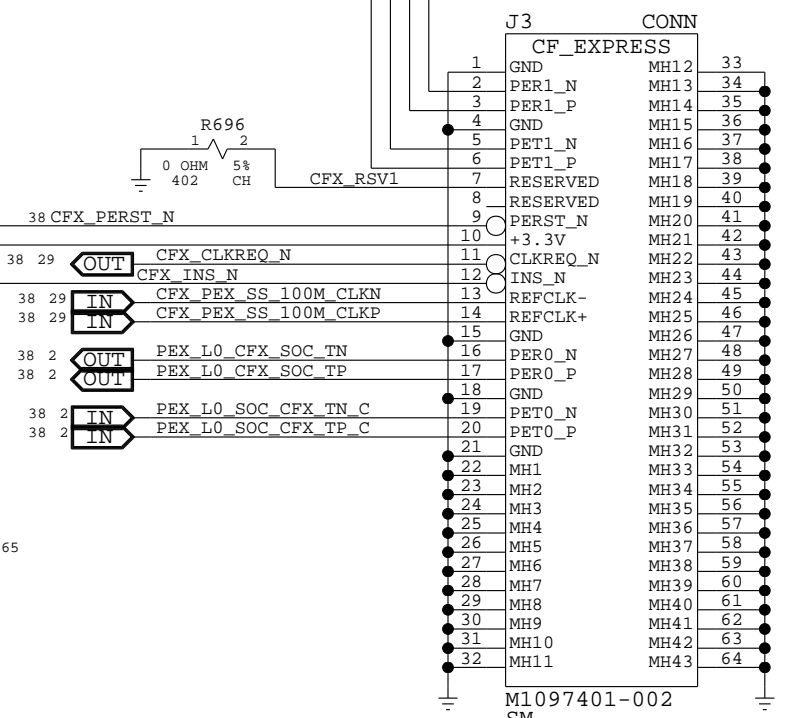
A



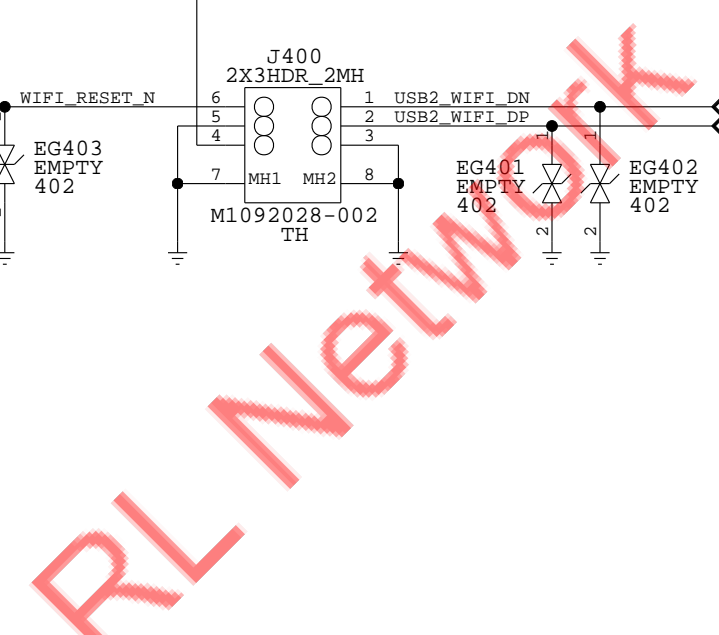
Q166 PROVIDES LOGIC INVERSION
SPDIF DETECT IS ACTIVE LOW
SOC REQUIRES ACTIVE HIGH



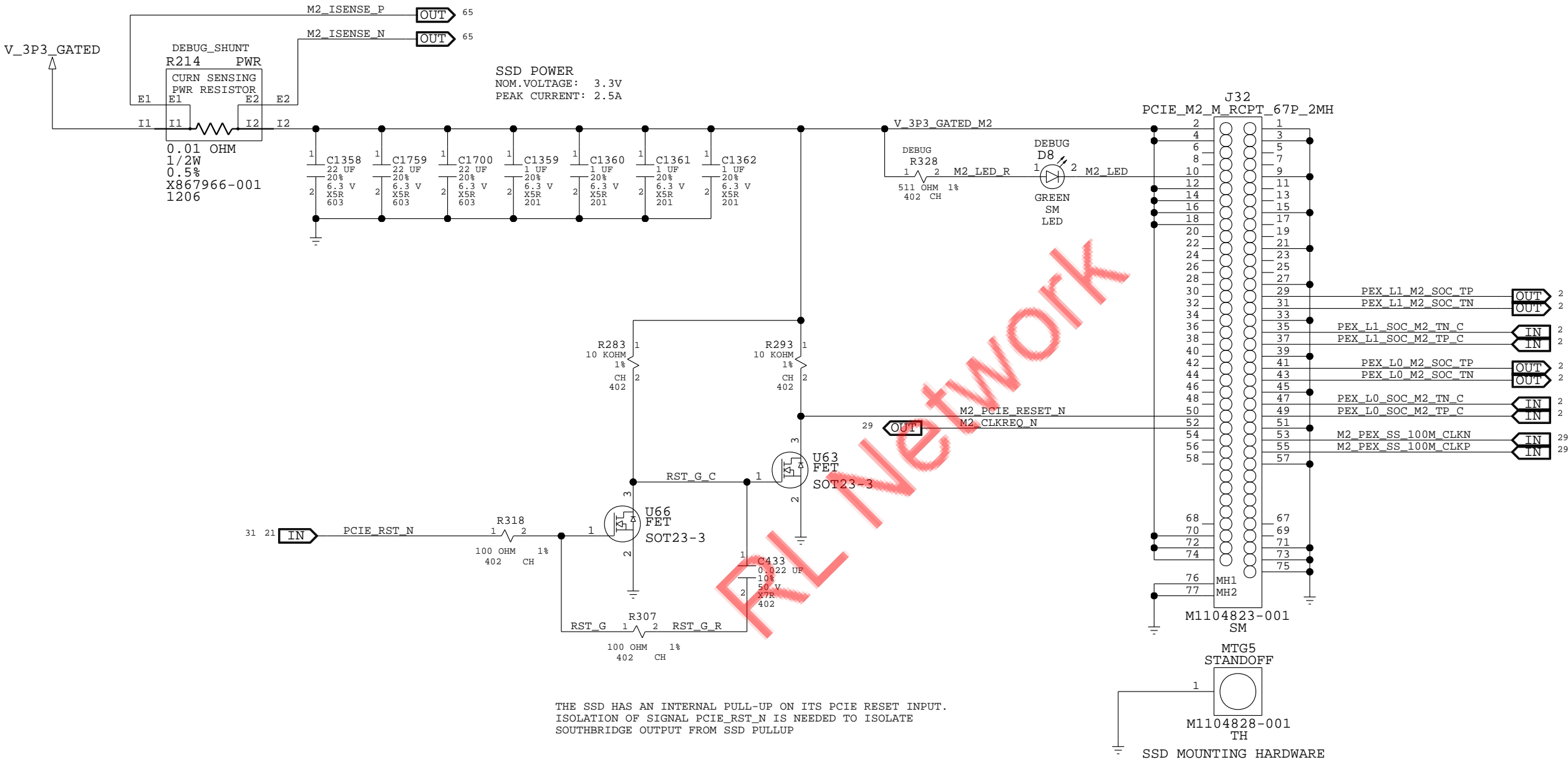
CFEXPRESS
2.5A EDC
1.55A TDC



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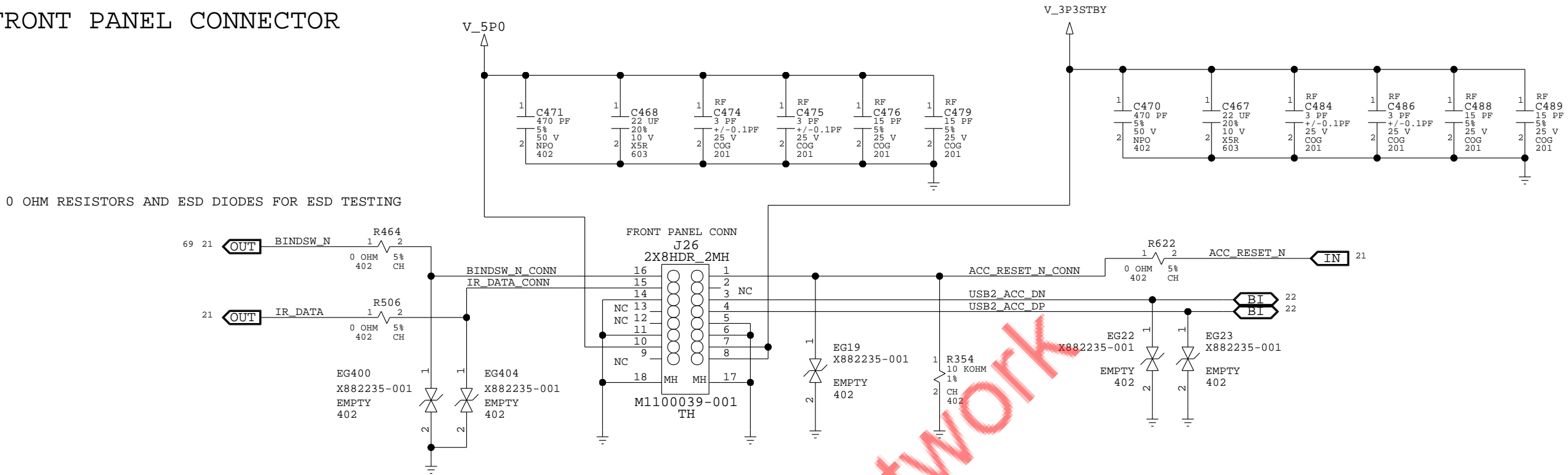
CONN: M.2



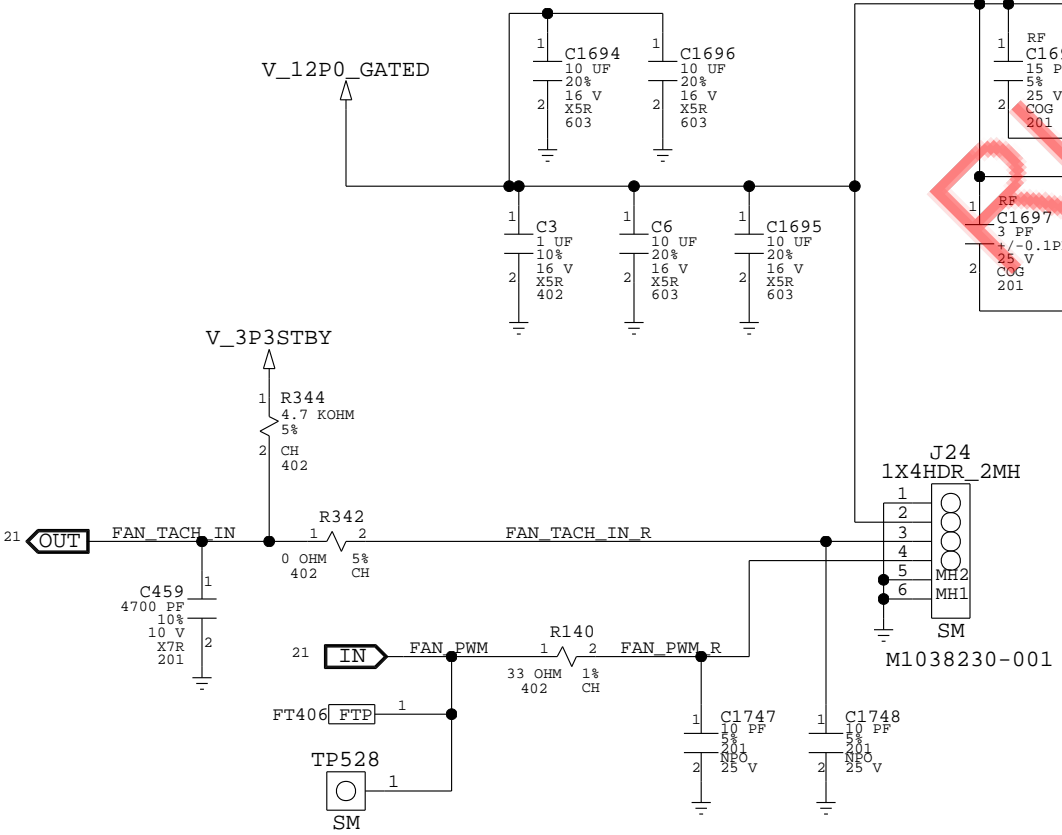
8		7		6		5		4		3		2		1	
CONN: ODD															
PLACEHOLDER FOR OBSOLETE ODD CIRCUITRY															
RL Network															
MICROSOFT CONFIDENTIAL															
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CSA PAGE 42/76															
FAB C															
VER 0.12															
8		7		6		5		4		3		2		1	

CONN: FRONT PANEL, FAN, NEXUS

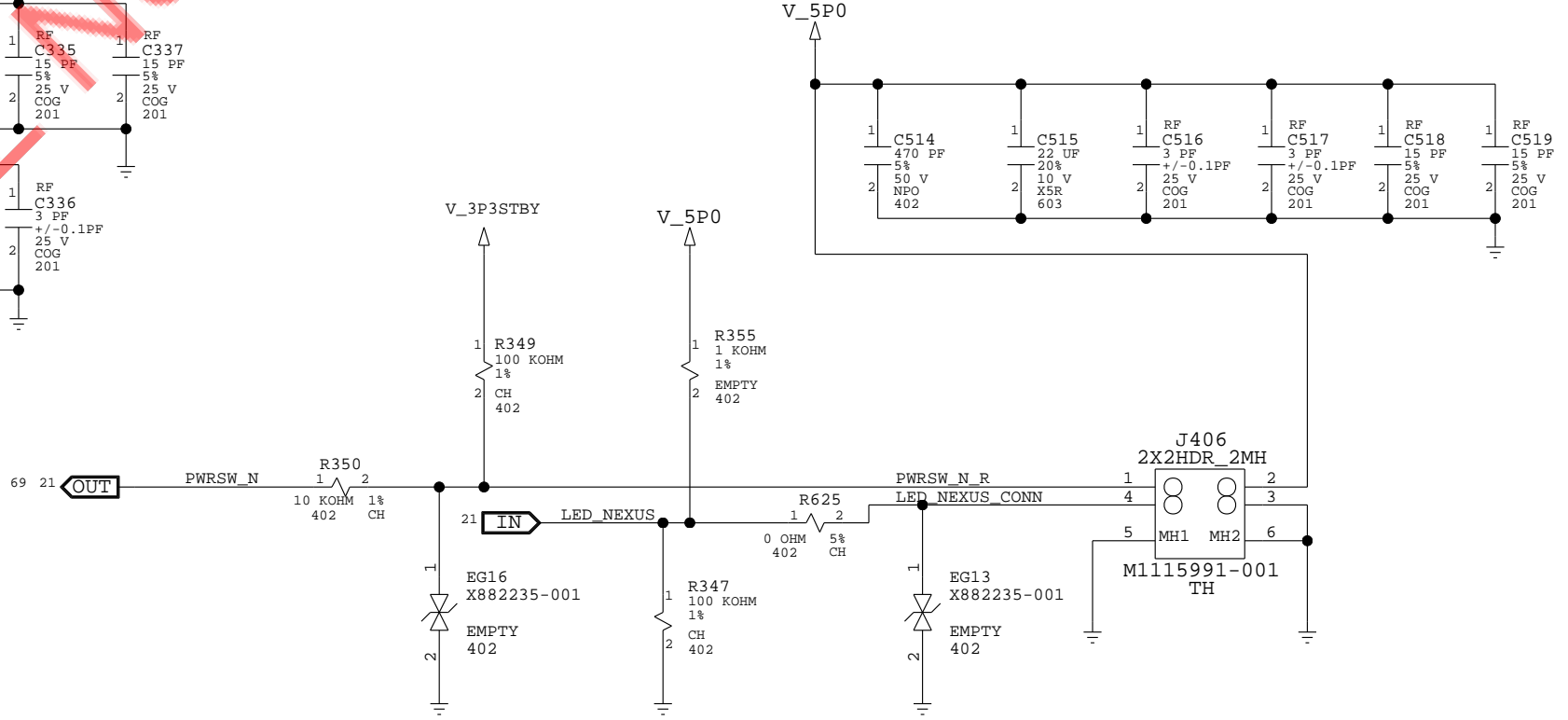
FRONT PANEL CONNECTOR



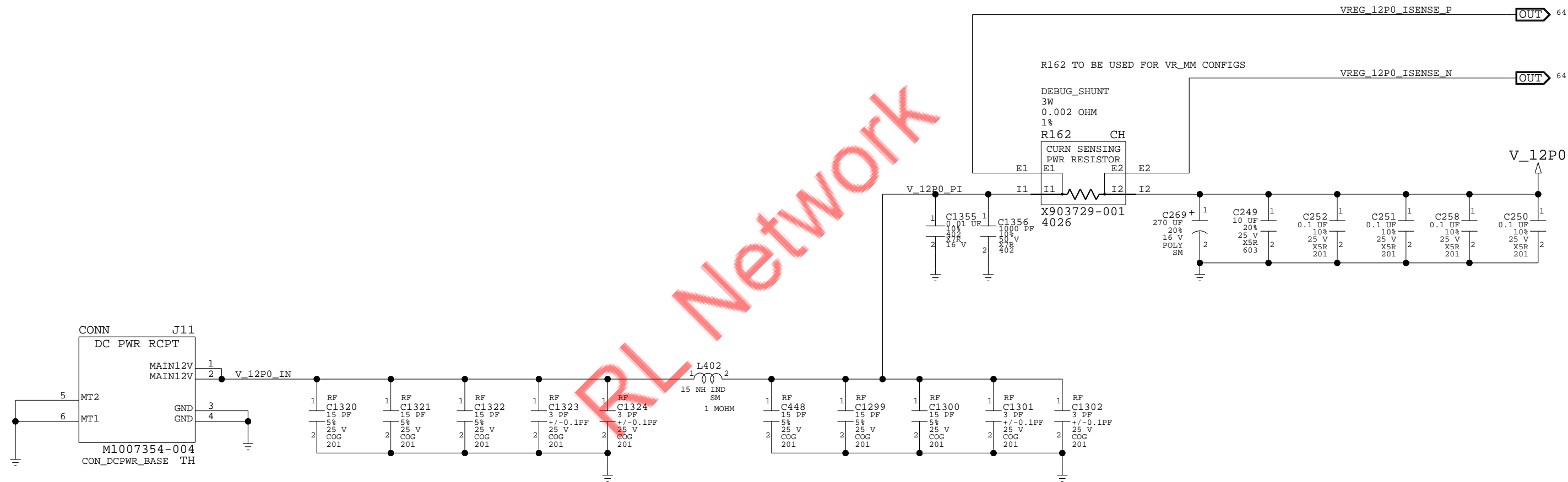
FAN CONNECTOR



NEXUS CONNECTOR

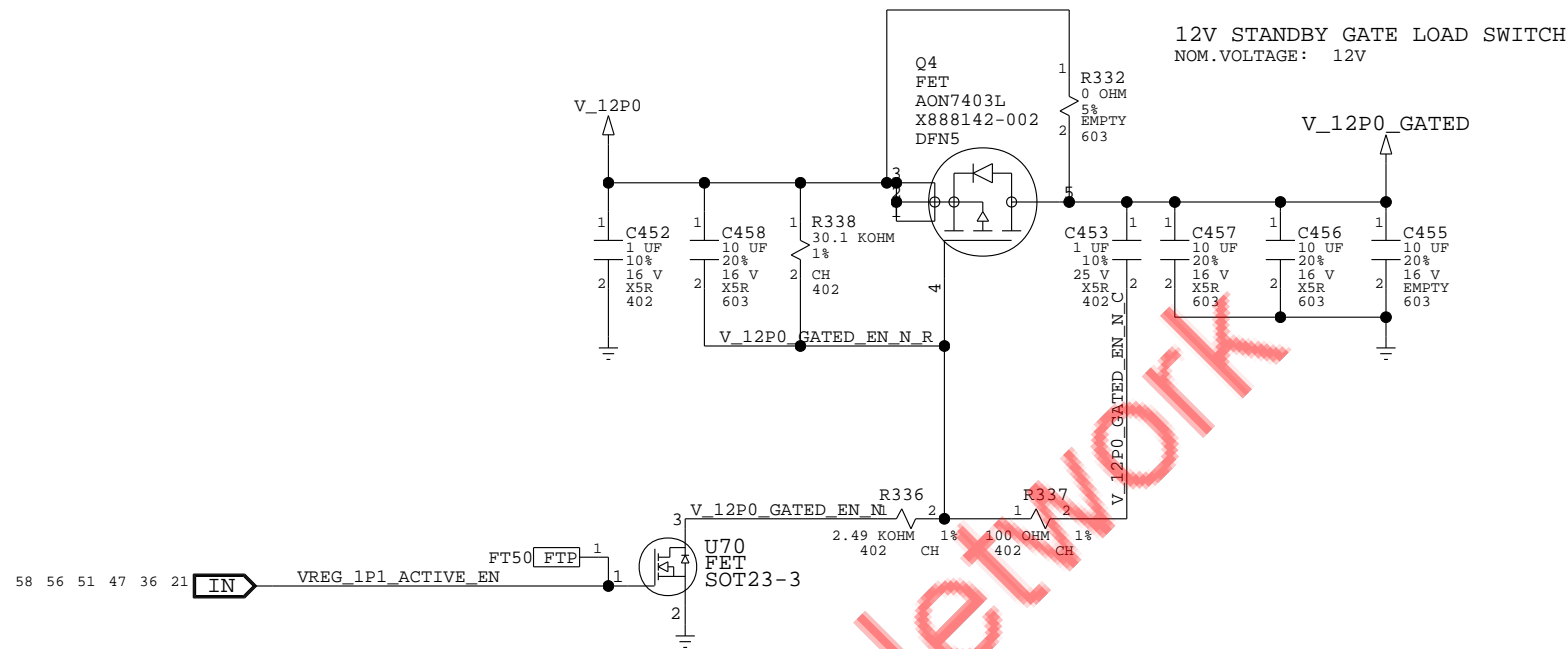


CONN: POWER



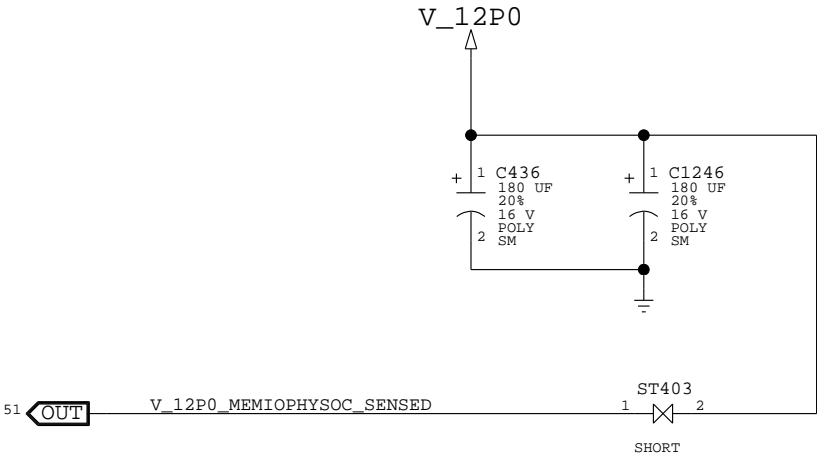
MXXXXXXX-001	MATL	REF	DES	DESCR.	BOM PROPERTY
M1007354-004	CONN	J11	FOXCONN DC POWER CONNECTOR 1ST MAT SRC	CON_DCPWR_FOXC_1	
M1021821-003	CONN	J11	FOXLINK QUAL DC POWER CONN 1ST MAT SRC	CON_DCPWR_FOXL_1	
M1040539-001	CONN	J11	FOXCONN QUAL DC POWER CONN 2ND MAT SRC	CON_DCPWR_FOXC_2	
M1040540-001	CONN	J11	FOXLINK QUAL DC POWER CONN 2ND MAT SRC	CON_DCPWR_FOXL_2	

VREGS: V_12P0_GATED

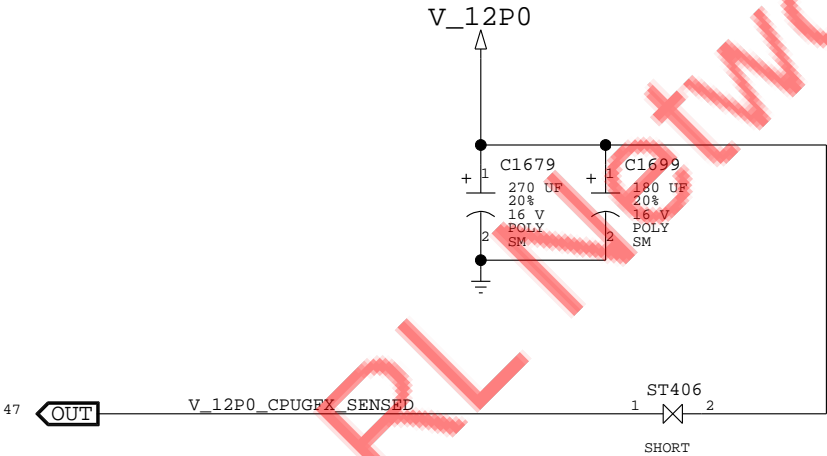


VREGS: INPUT DECOUPLING

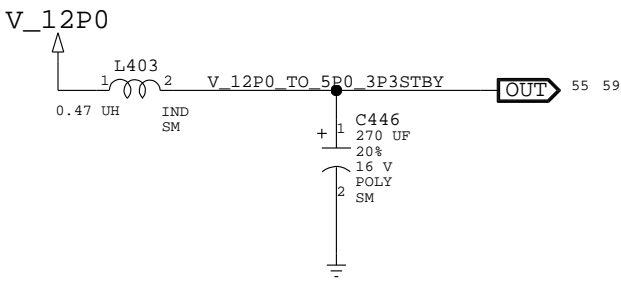
CPU/MEMIO/MEMPHY/SOC INPUT FILTER



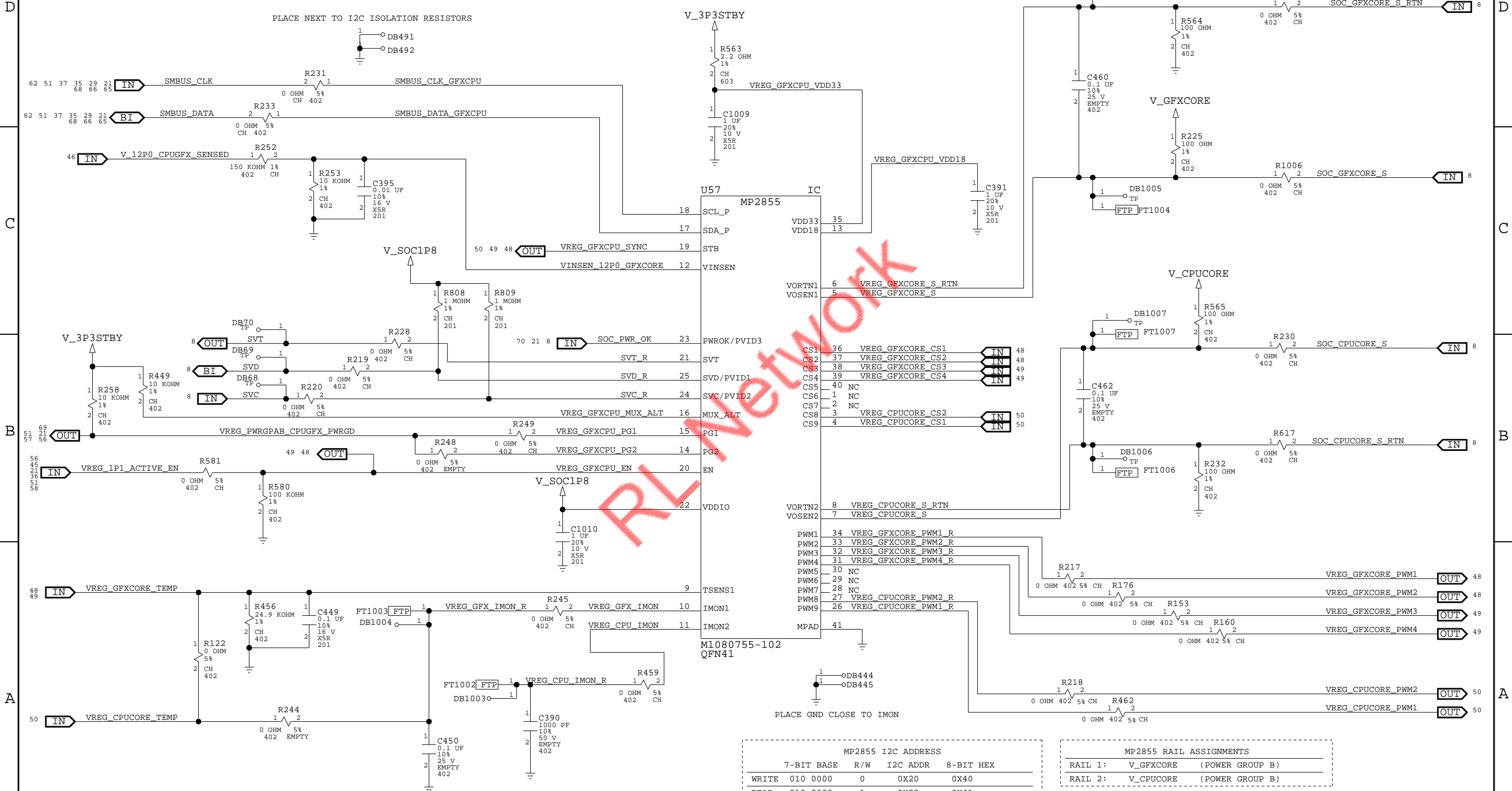
GFX INPUT FILTER



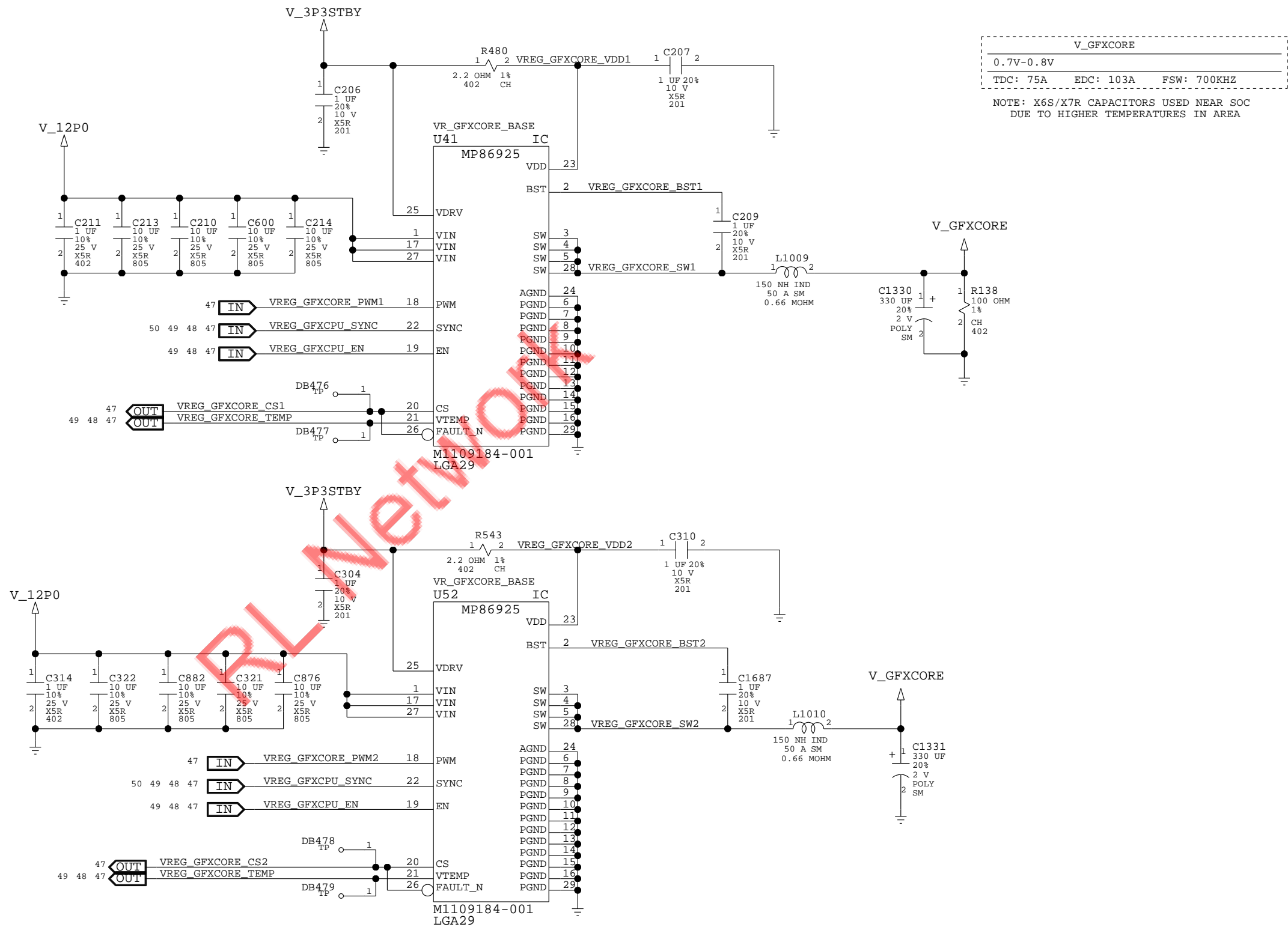
5P0 AND 3P3STBY INPUT FILTER



VREGS: V_CPUCORE, V_GFXCORE CONTROLLER



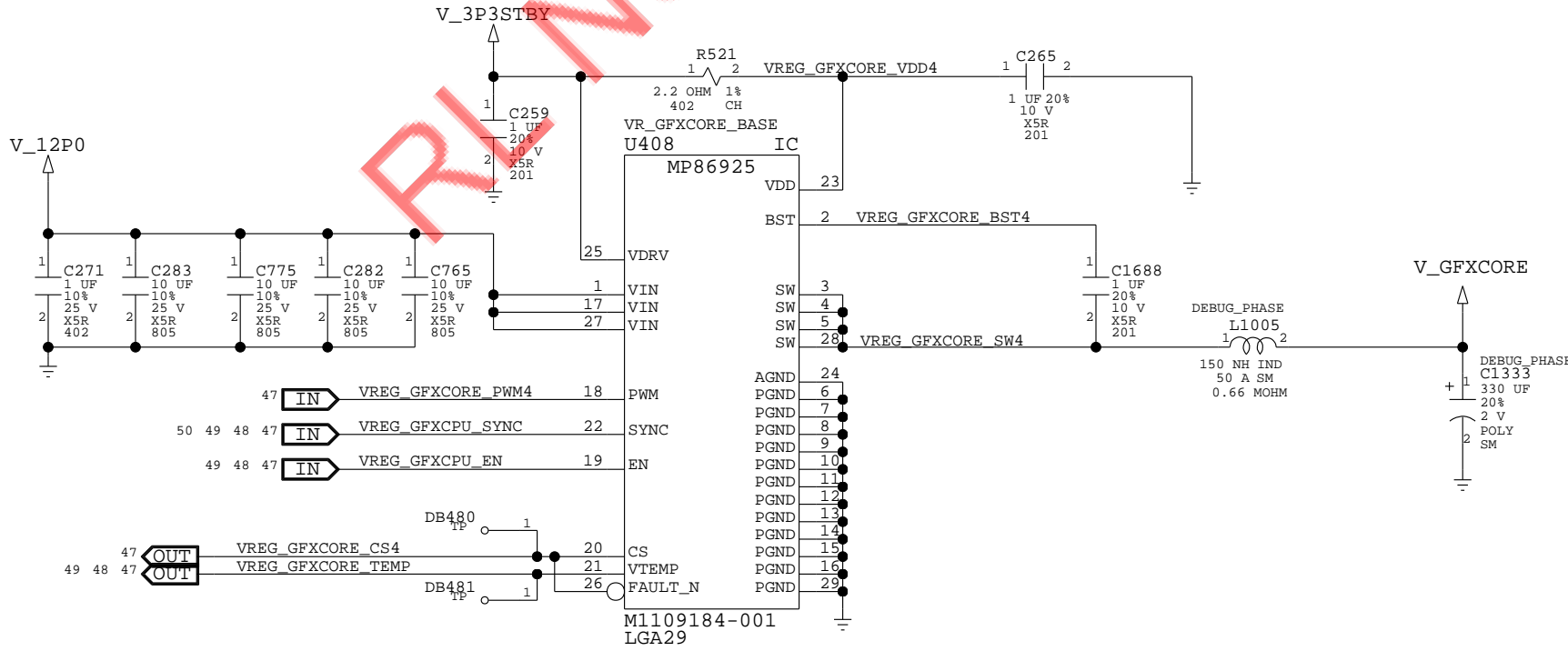
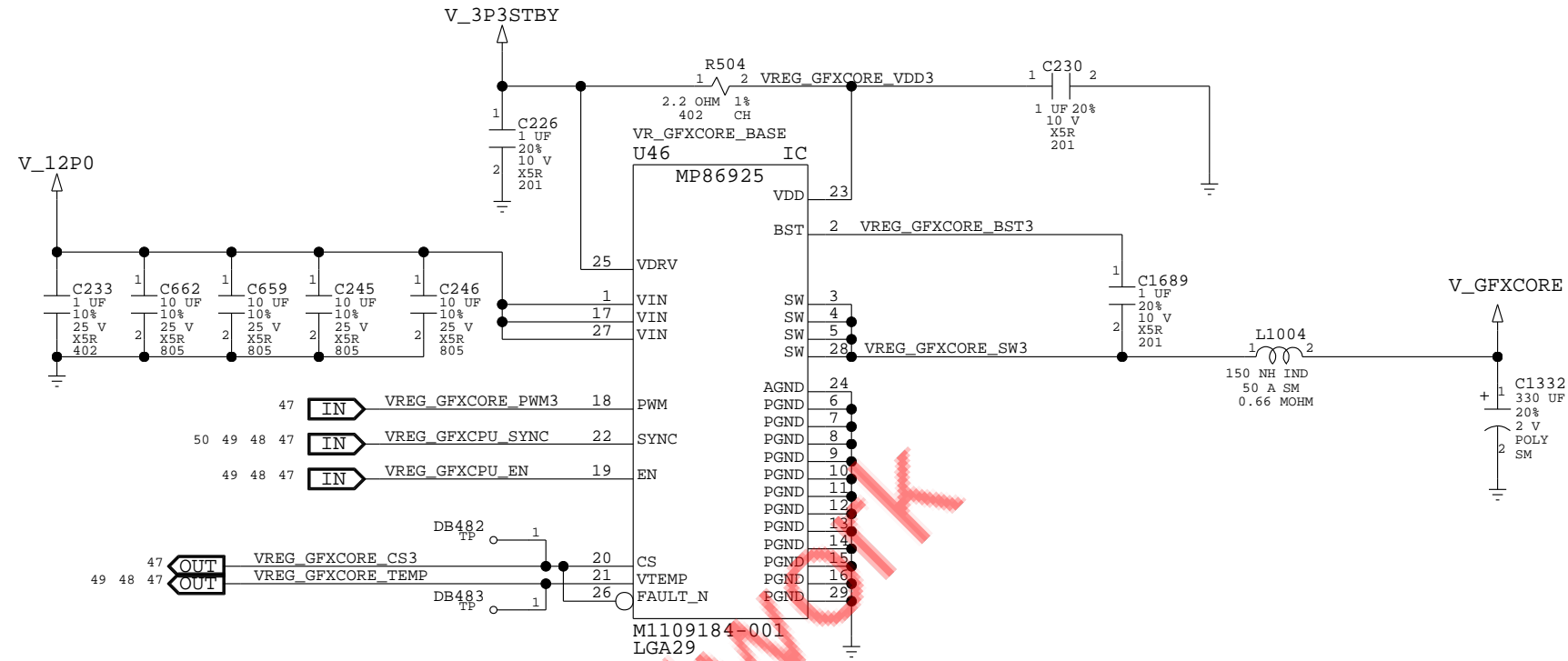
VREGS: V_GFXCORE OUTPUT PHASE 1 & 2



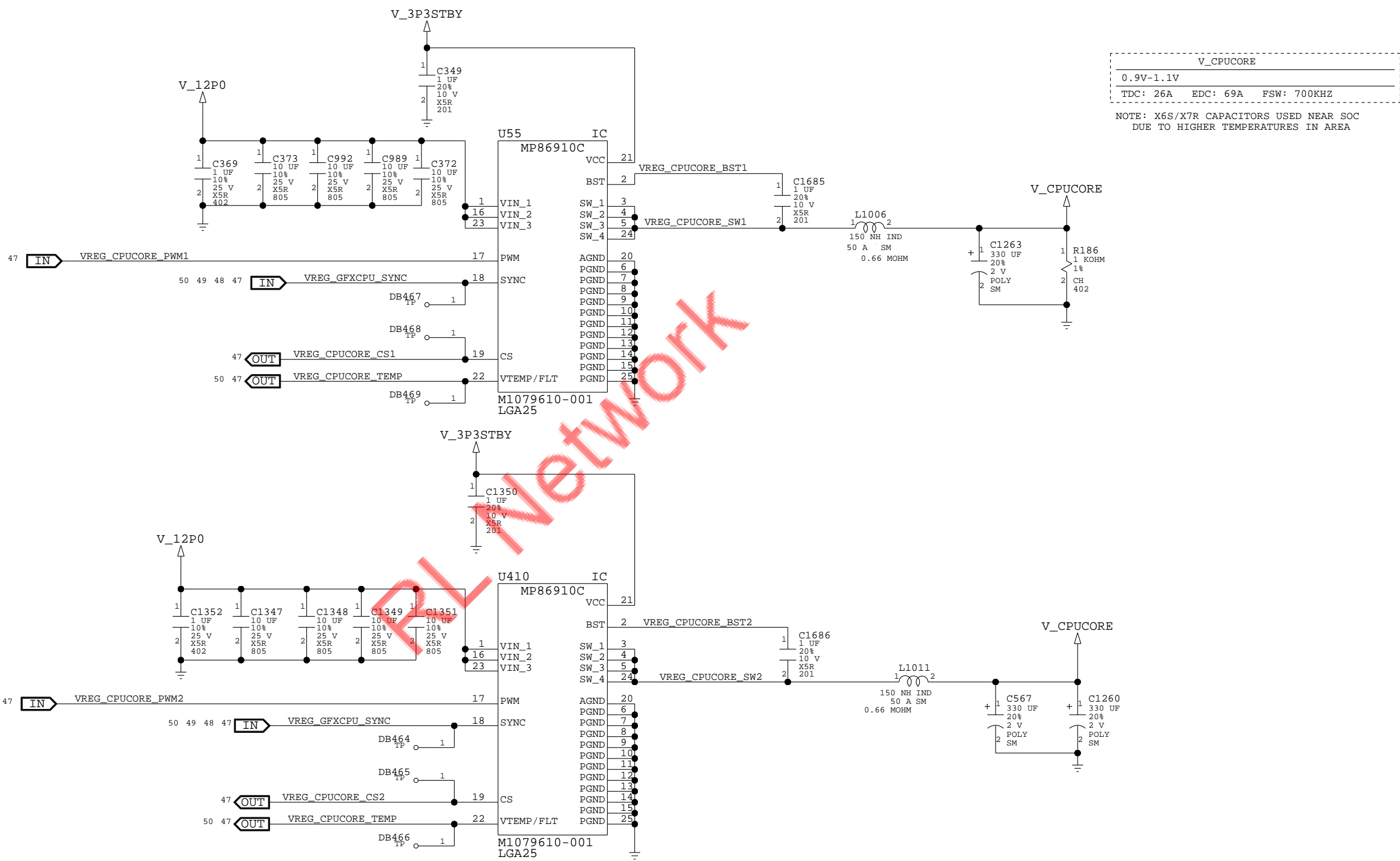
MXXXXXXX-001	MATL	REF DES	DESCR.	BOM PROPERTY
M1109184-001	IC	U41, U52, U46, U408	IC-PWR, DC/DC CONV, MP86925	VR_GFXCORE_MP86925
M1079609-001	IC	U41, U52, U46, U408	IC-PWR, DC/DC CONV, MP86915	VR_GFXCORE_MP86915
M1109184-001	IC	U41, U52, U46	IC-PWR, DC/DC CONV, MP86925	VR_GFXCORE_RETAIL

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VREGS: V_GFXCORE OUTPUT PHASE 3 & 4



VREGS: V_CPUCORE OUTPUT



VREGS: V_MEMIO, V_MEMPHY, V_SOC CONTROLLER

D

D

C

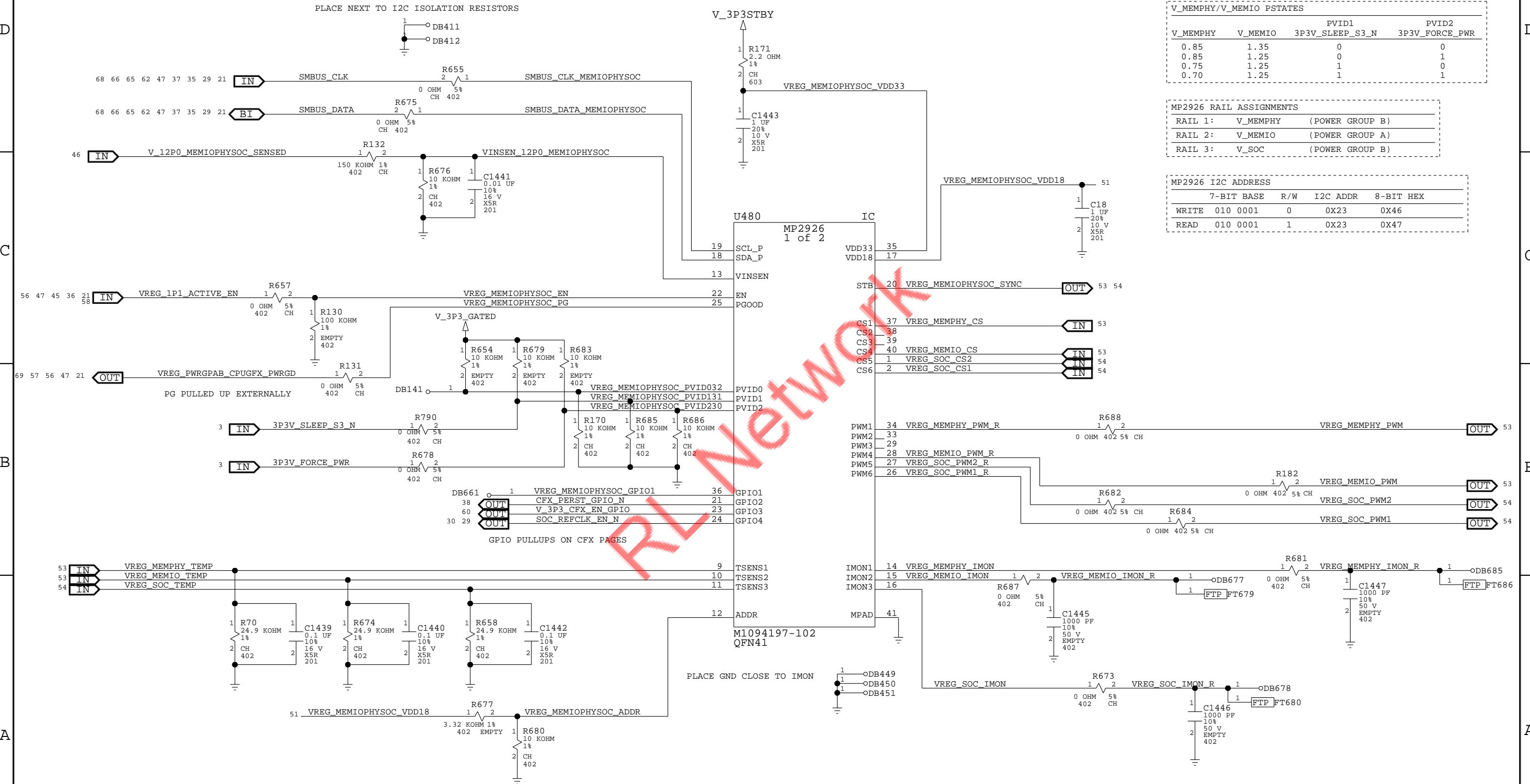
C

B

B

A

A



V_MEMPHY/V_MEMIO PSTATES				
V_MEMPHY	V_MEMIO	3P3V_SLEEP_S3_N	3P3V_FORCE_PWR	
0.85	1.35	0	0	
0.85	1.25	0	1	
0.75	1.25	1	0	
0.70	1.25	1	1	

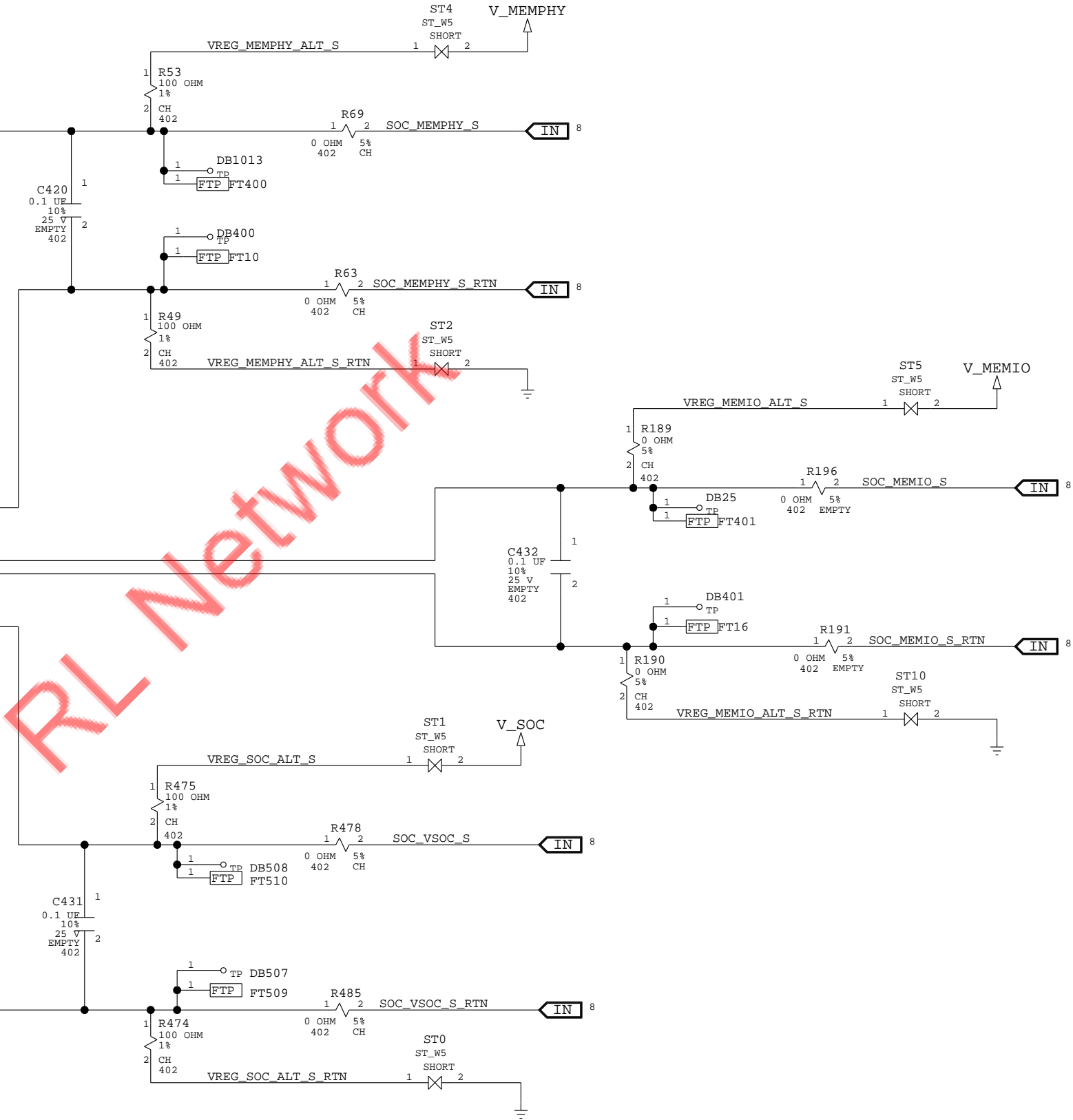
MP2926 RAIL ASSIGNMENTS		
RAIL 1:	V_MEMPHY	(POWER GROUP B)
RAIL 2:	V_MEMIO	(POWER GROUP A)
RAIL 3:	V_SOC	(POWER GROUP B)

MP2926 I2C ADDRESS				
	7-BIT BASE	R/W	I2C ADDR	8-BIT HEX
WRITE	010 0001	0	0X23	0X46
READ	010 0001	1	0X23	0X47

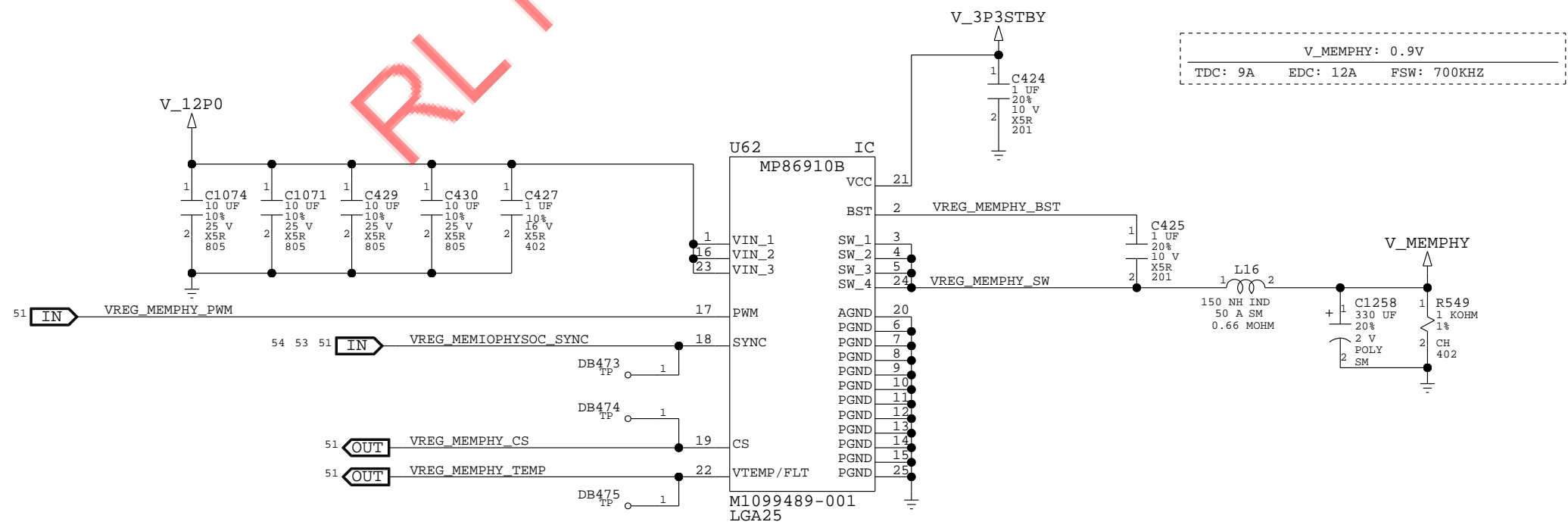
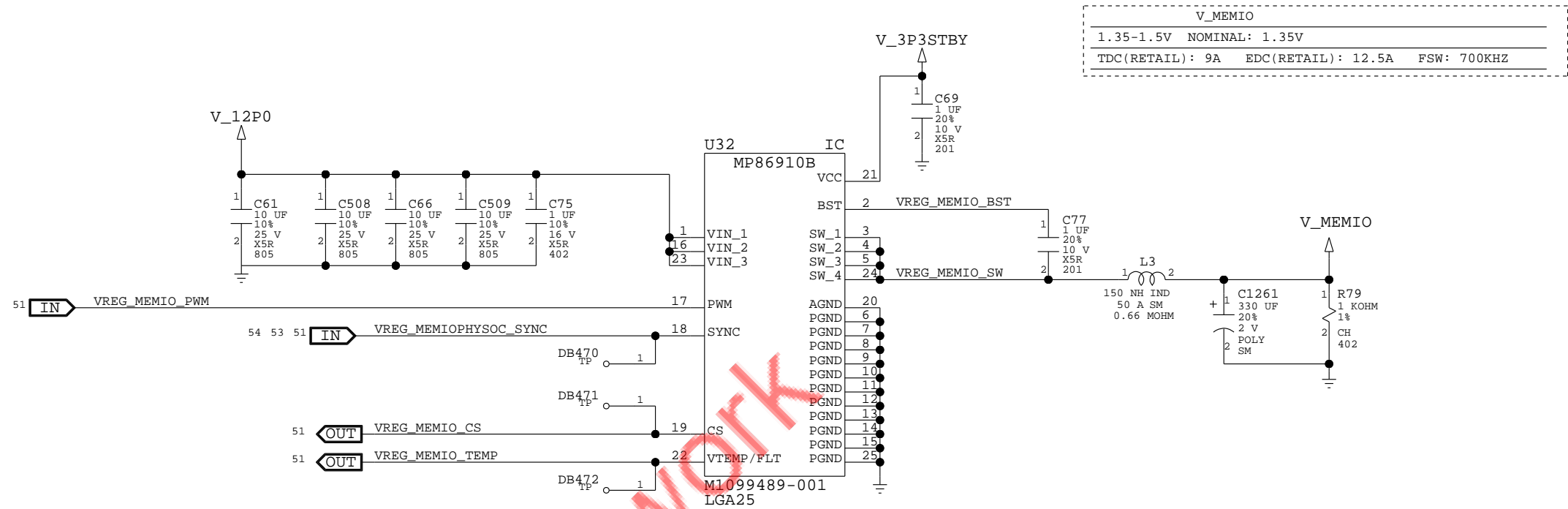
VREGS: V_MEMPIO, V_MEMPHY, V_SOC SENSE

MP2926 RAIL ASSIGNMENTS		
RAIL 1:	V_MEMPHY	(POWER GROUP B)
RAIL 2:	V_MEMPIO	(POWER GROUP A)
RAIL 3:	V_SOC	(POWER GROUP B)

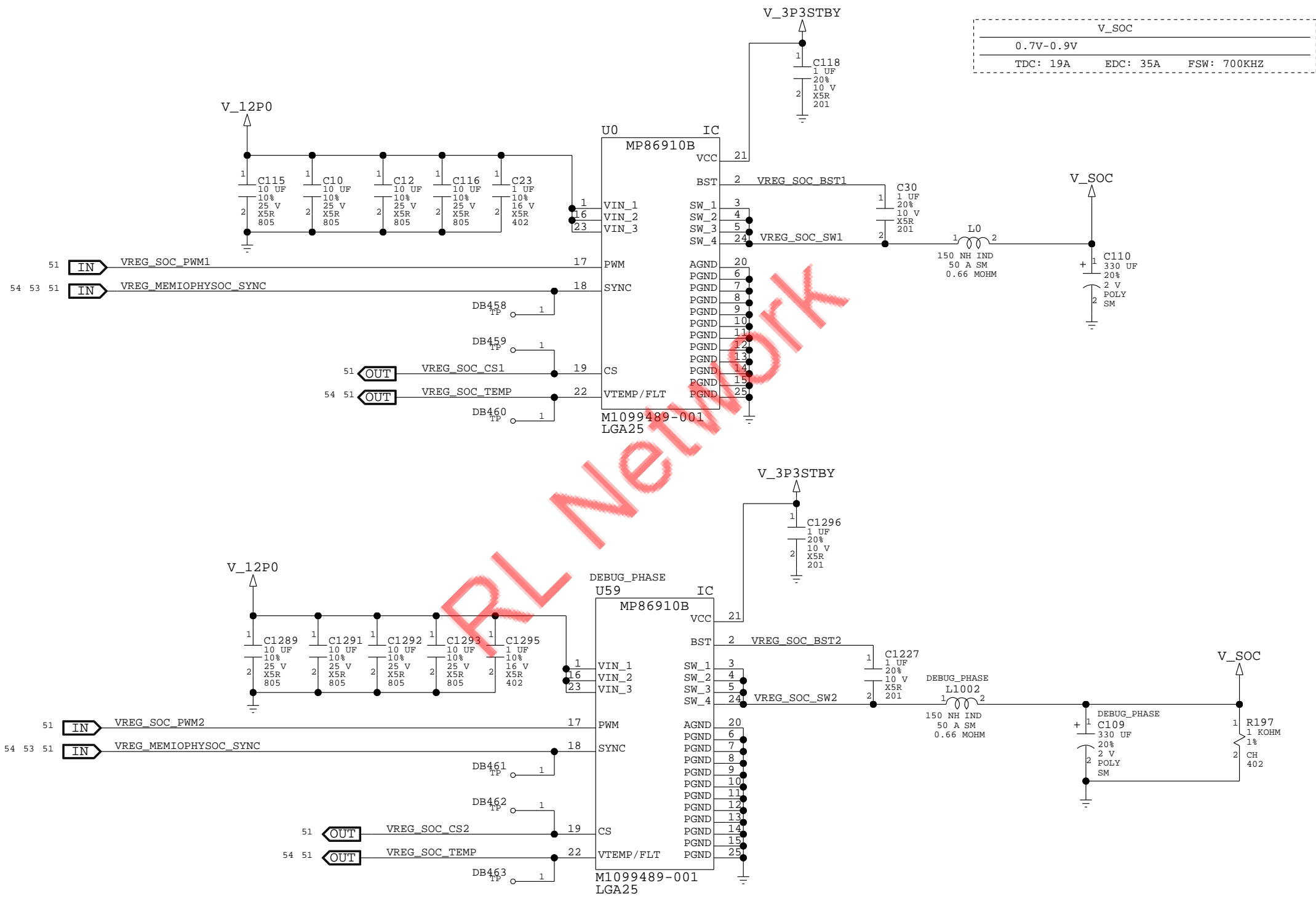
QFN41		M1094197-102	
2 of 2			
VOSEN1	3	VREG_MEMPHY_S	
VORTN1	4	VREG_MEMPHY_S_RTN	
VOSEN2	5	VREG_MEMPIO_S	
VORTN2	6	VREG_MEMPIO_S_RTN	
VOSEN3	7	VREG_SOC_S	
VORTN3	8	VREG_SOC_S_RTN	
MP2926		U480 IC	



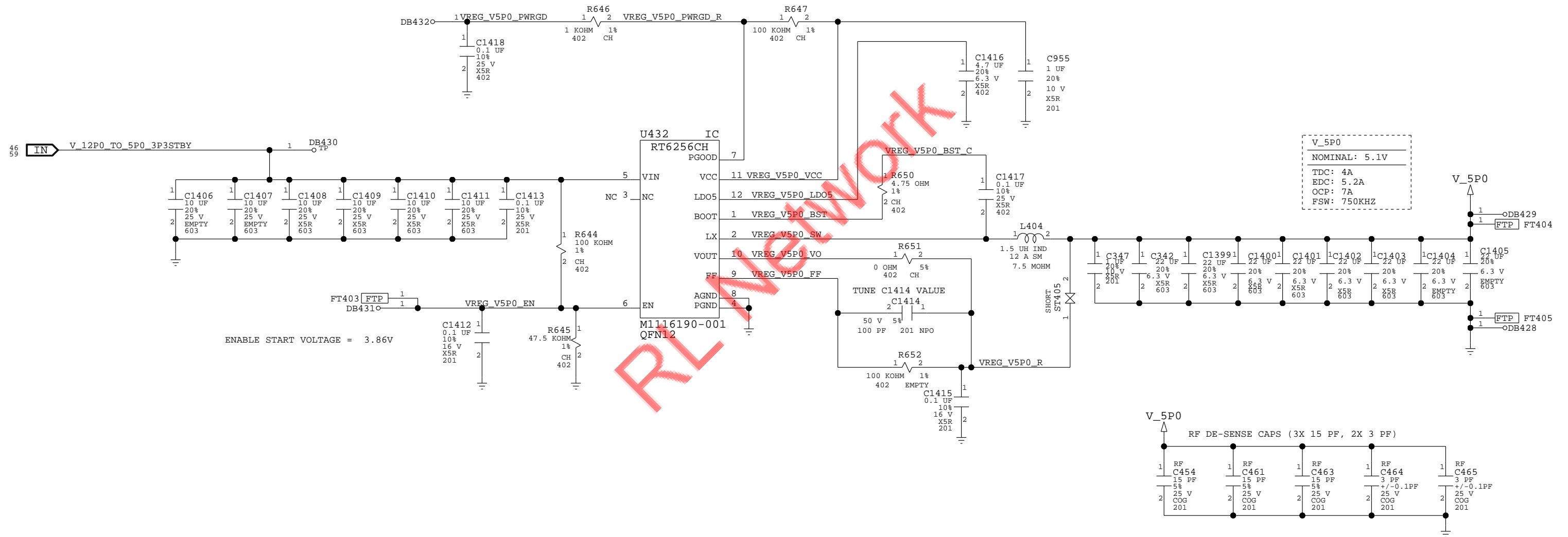
VREGS: V_MEMIO AND V_MEMPHY OUTPUT



VREGS: V_SOC OUTPUT

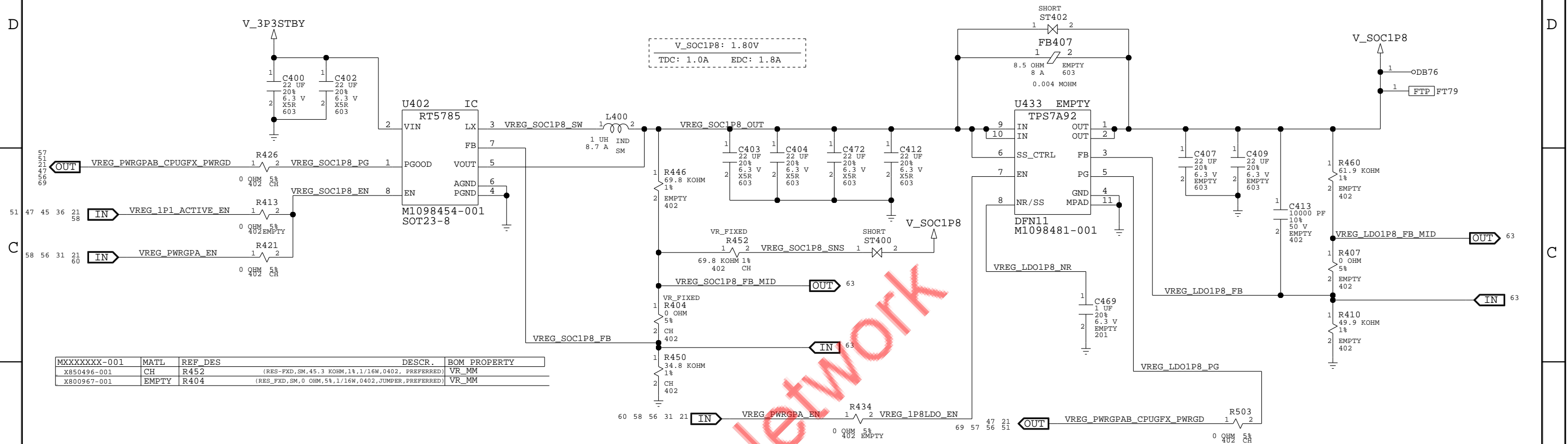


```
VREGS:  V_5P0
```

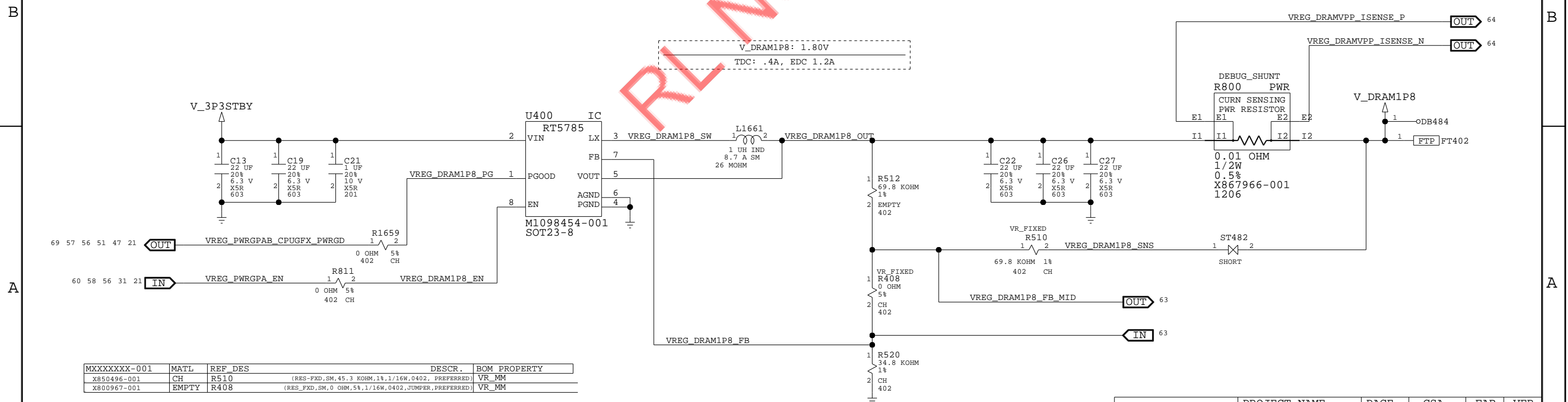


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```
VREGS:  V_SOC1P8,  V_DRAM1P8
```



MXXXXXXX-001	MATL	REF DES	DESCR.	BOM PROPERTY
X850496-001	CH	R452	(RES-FXD,SM,45.3 KOHM,1%,1/16W,0402, PREFERRED)	VR_MM
X800967-001	EMPTY	R404	(RES_FXD,SM,0 OHM,5%,1/16W,0402,JUMPER,PREFERRED)	VR_MM



XXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
X850496-001	CH	R510	(RES_FXD,SM,45.3 KOHM,1%,1/16W,0402, PREFERRED)	VR_MM
X800967-001	EMPTY	R408	(RES_FXD,SM,0 OHM,5%,1/16W,0402,JUMPER,PREFERRED)	VR_MM

VREGS: V_SOCPHY, V_FUSE

D

D

C

C

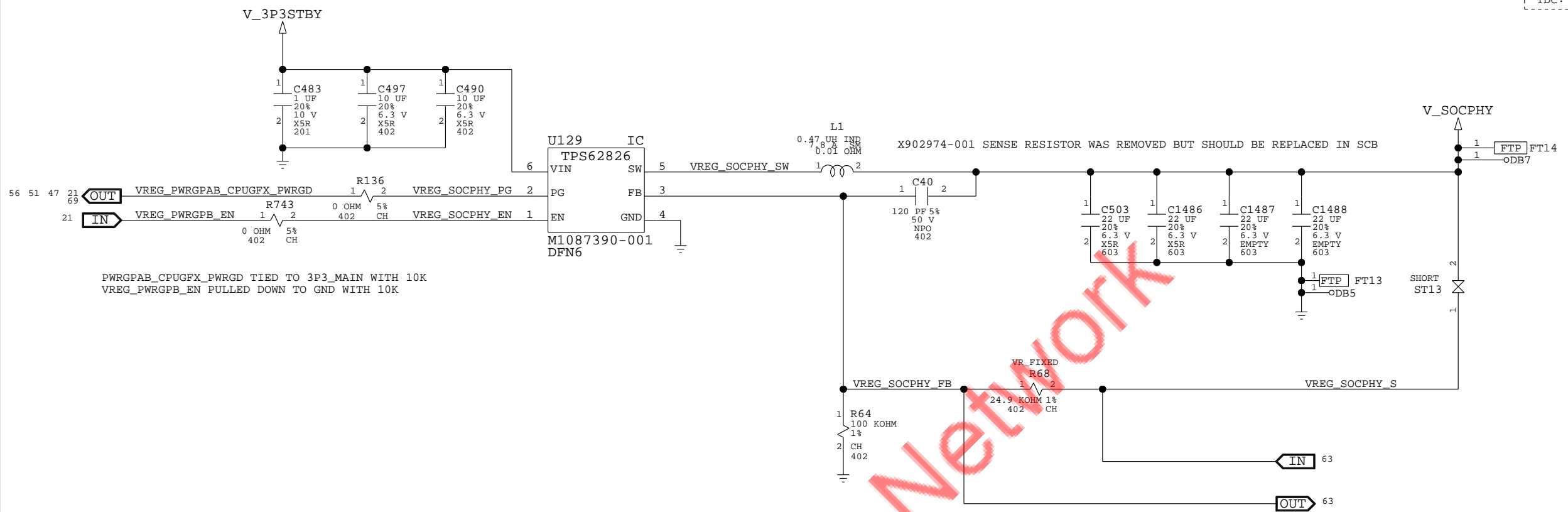
B

B

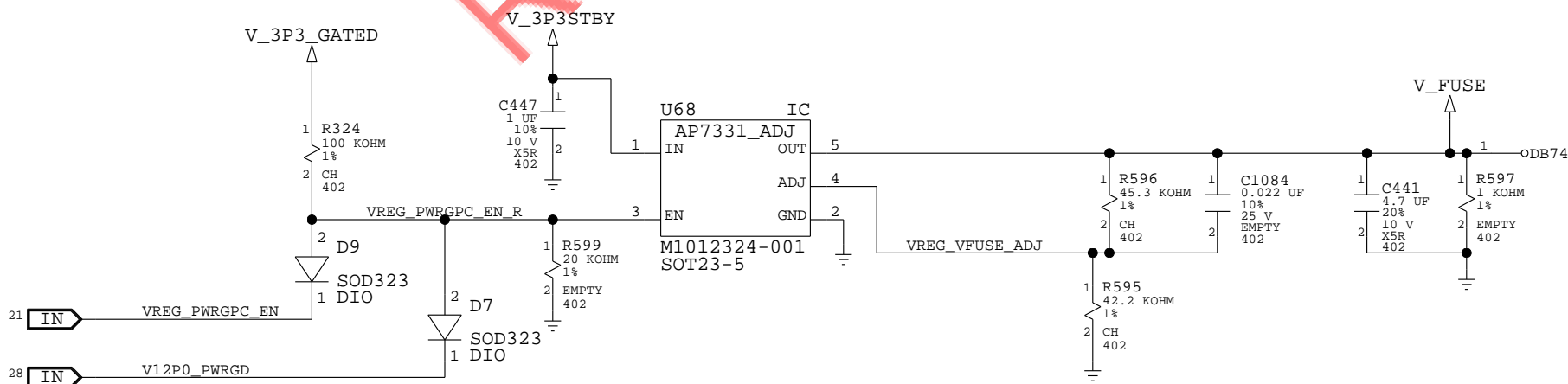
A

A

V_SOCPHY: 0.75V		
TDC: 1.3A	EDC: 3.4A	FSW: 2.2MHZ

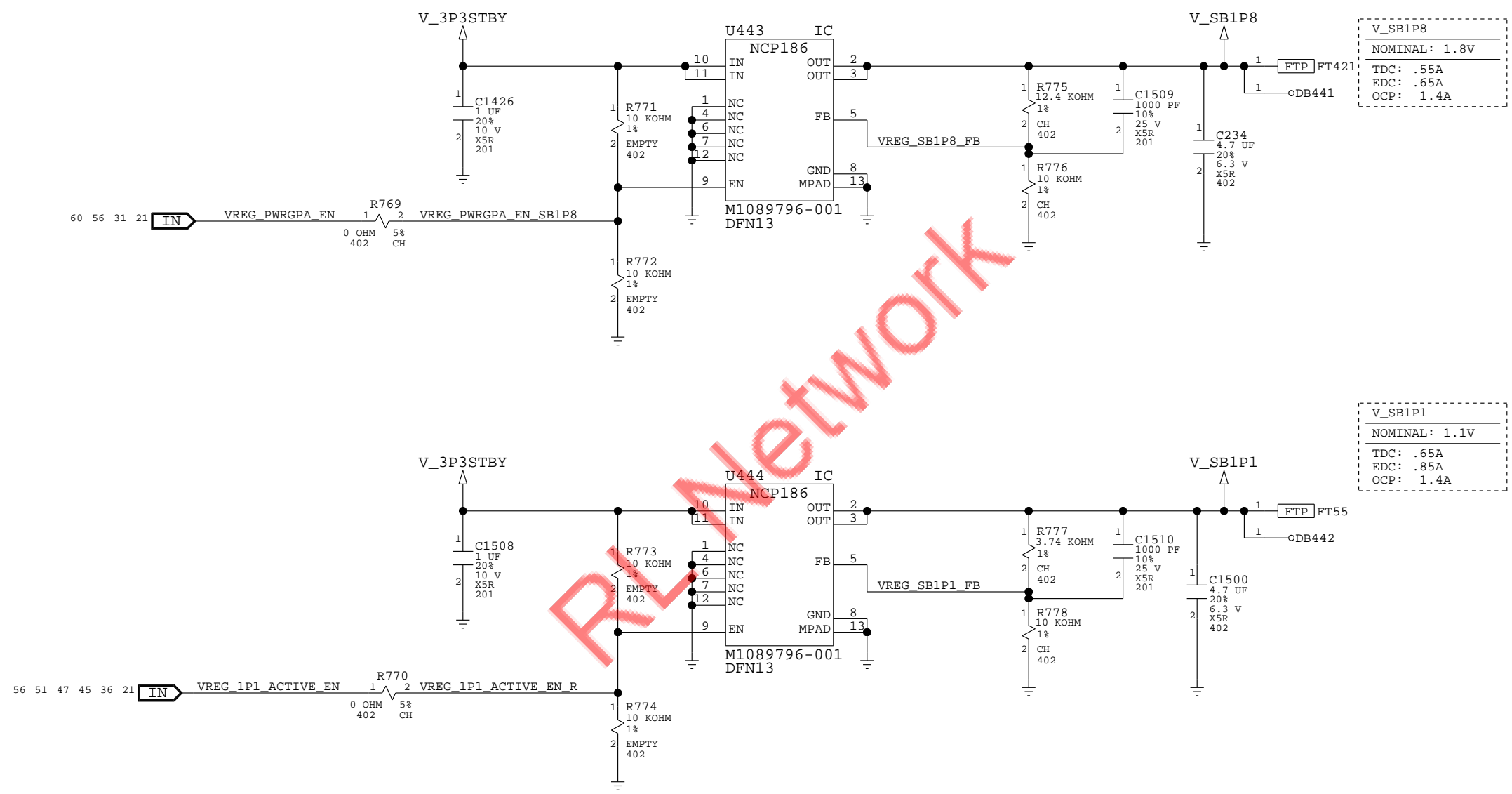


V_FUSE: 0.83V	
TDC: 100MA	



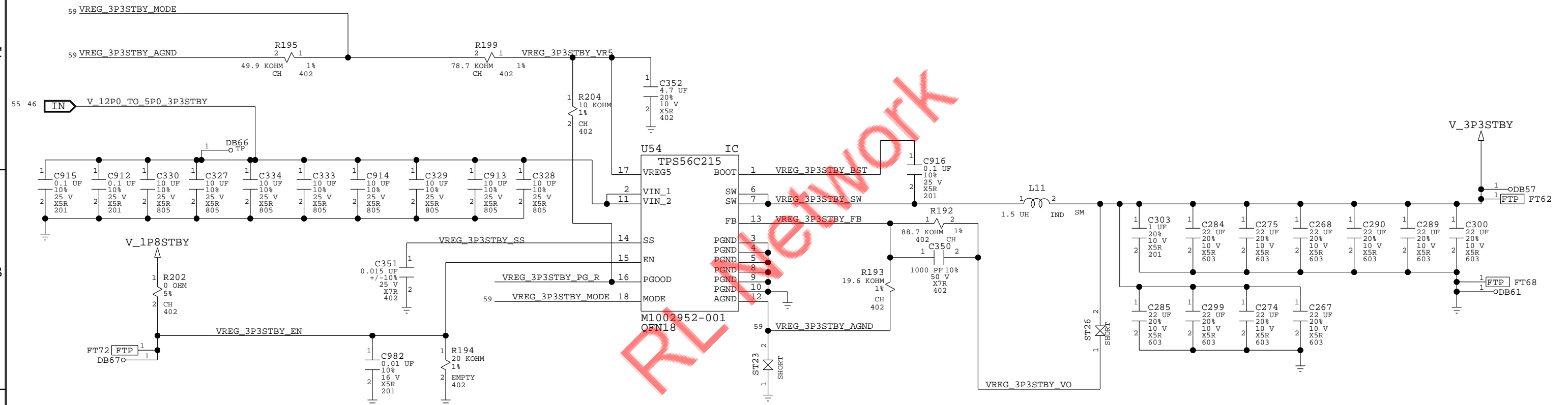
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VREGS: V_SB1P8, V_SB1P1

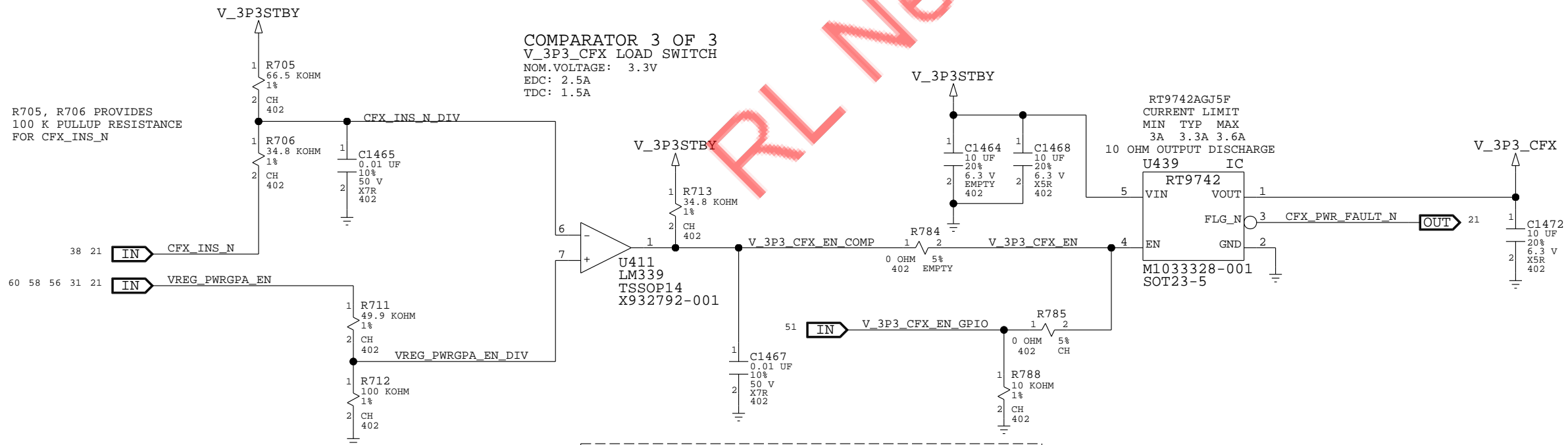


[illegible]

```
V_3P3STBY
NOM. VOLTAGE: 3.32
EST TDC = 9A
EST EDC = 12A
```

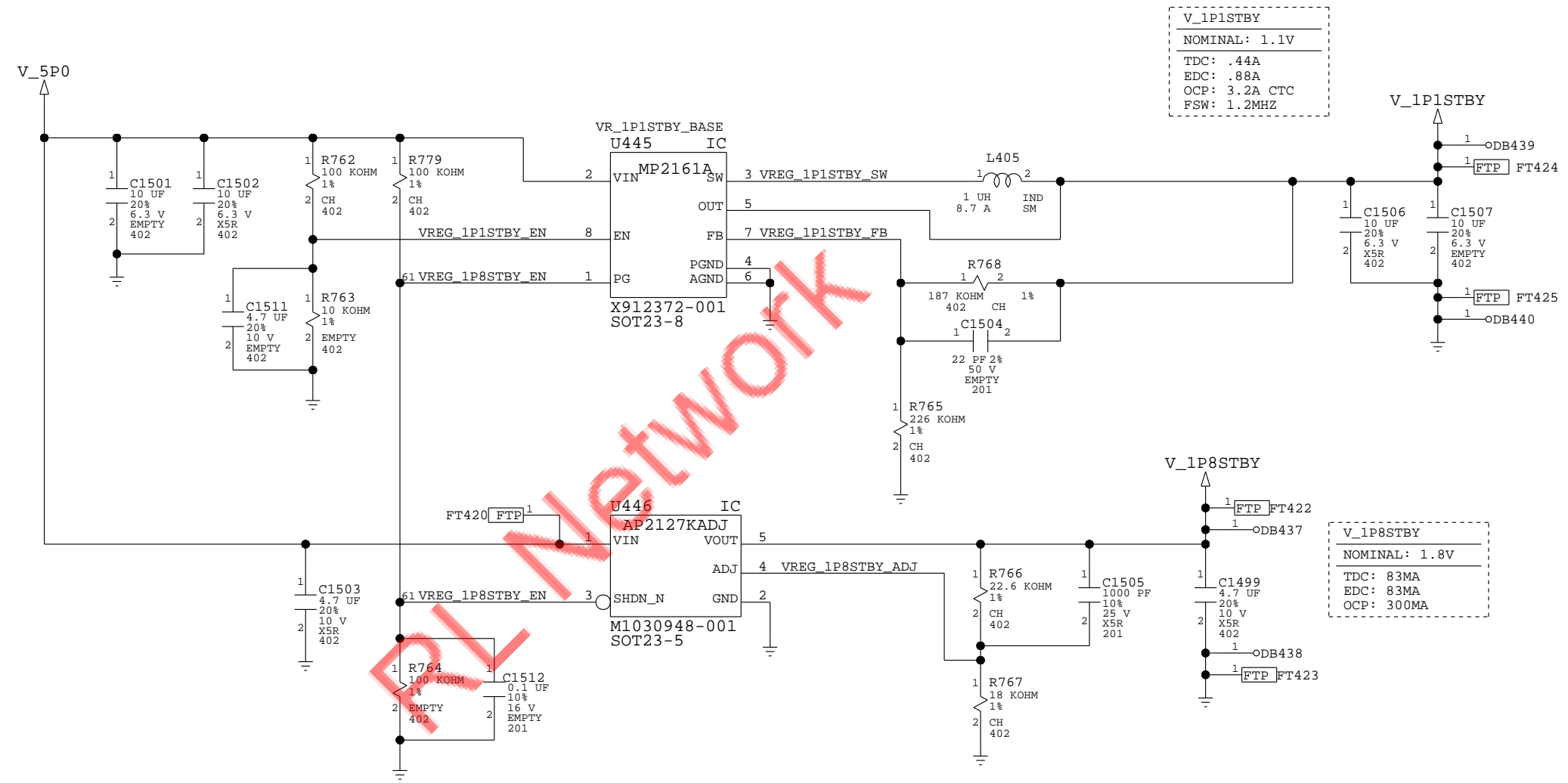


```
V_3P3_GATED POWERS M.2, SPDIF, SPI FLASH (SOC)
SOC VDD3, CLOCK GENERATOR 3.3V
```



GPA_EN	CFX_INS_N	GPA_EN_DIV	CFX_INS_N_DIV	ENABLE
3.3V	0V	2.2V	1.13V	3.3V
3.3V	3.3V	2.2V	3.3V	0V
0V	0V	0V	1.13V	0V
0V	3.3V	0V	3.3V	0V

VREGS: V_1P1STBY, V_1P8STBY

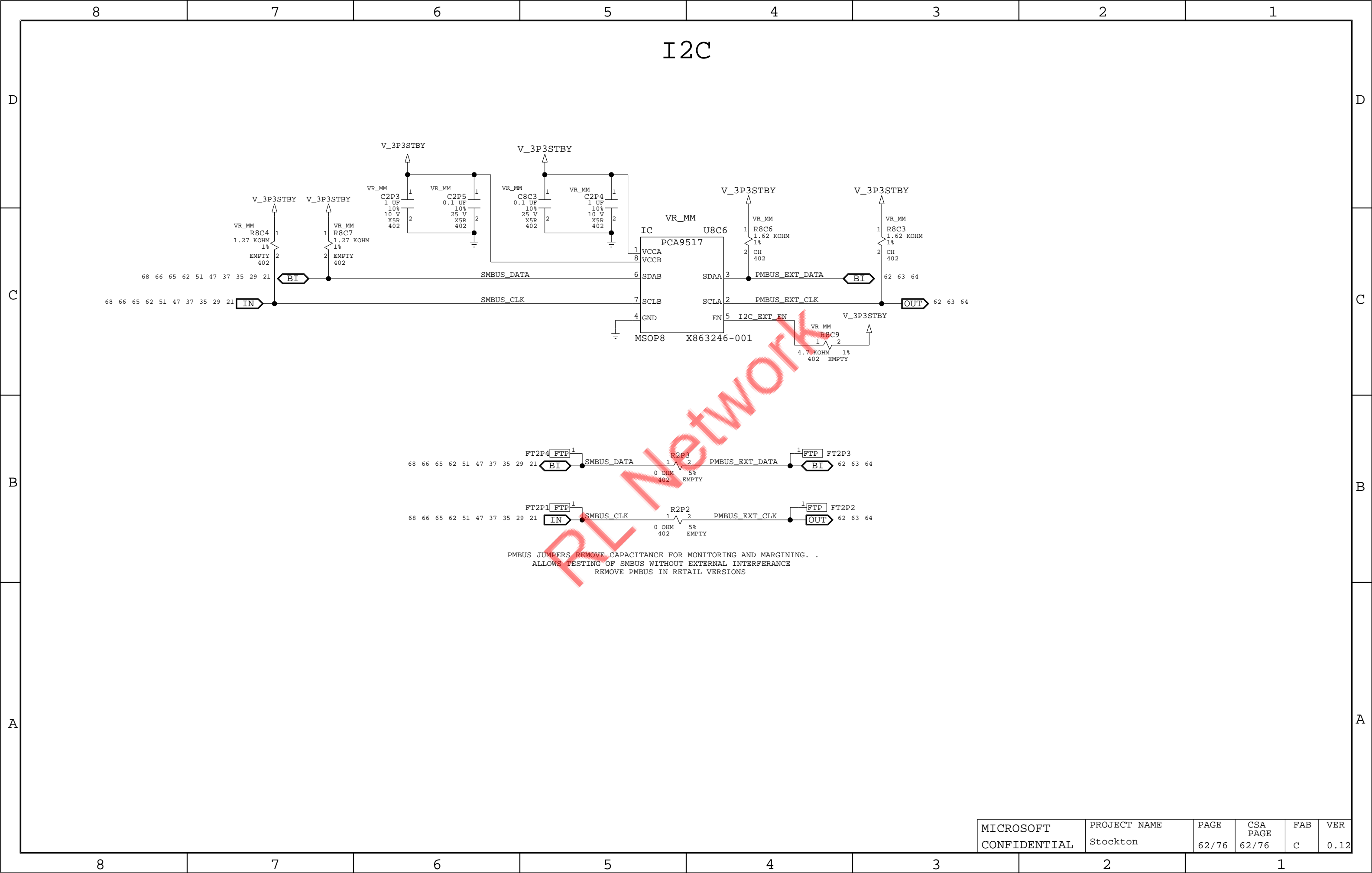


V_1P1STBY
NOMINAL: 1.1V
TDC: .44A
EDC: .88A
OCP: 3.2A CTC
FSW: 1.2MHZ

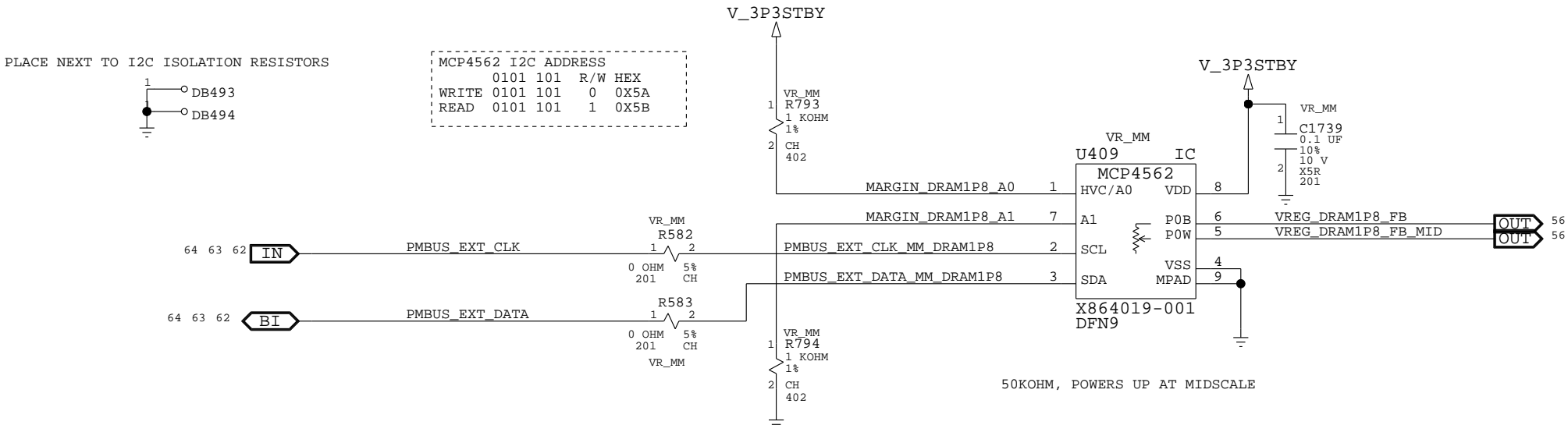
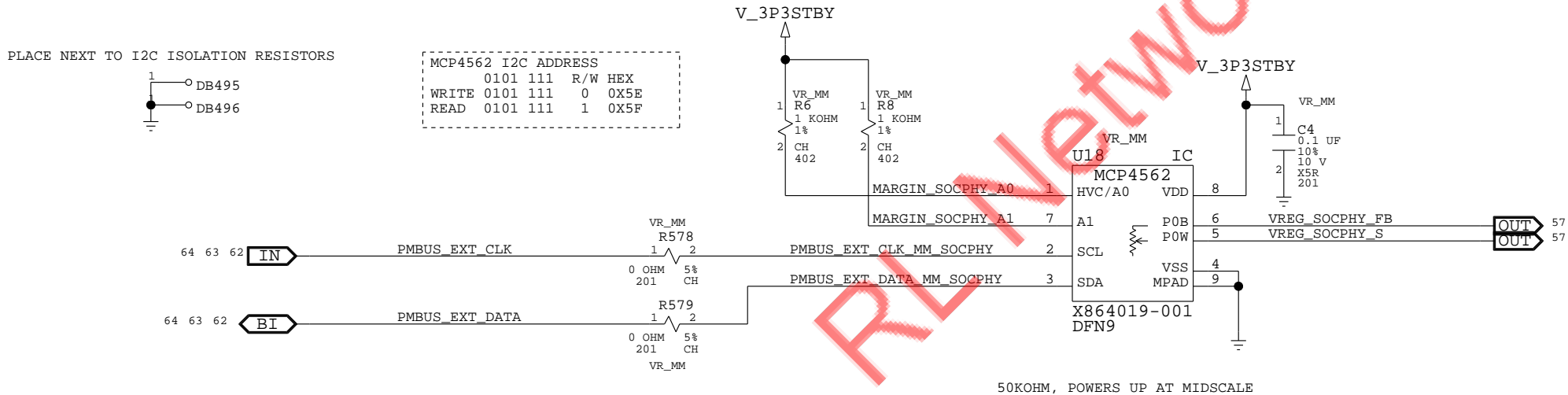
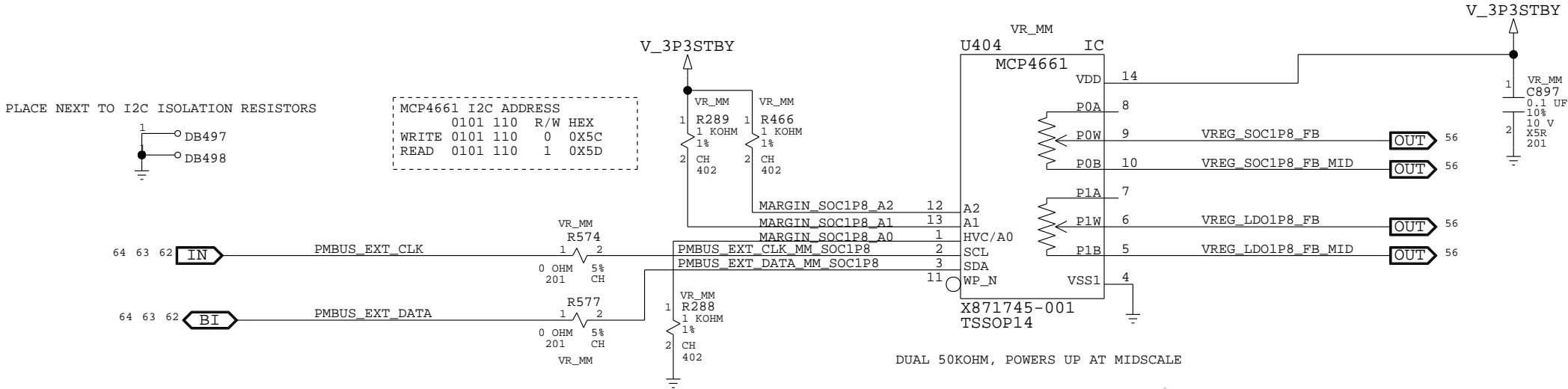
V_1P8STBY
NOMINAL: 1.8V
TDC: 83MA
EDC: 83MA
OCP: 300MA

MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
X912372-001	IC	U445	IC-PWR,VREG,SM,TSOT23-8,STEP DOWN,6V,2A,MP2161A	VR_1P1STBY_MPS
M1018565-001	IC	U445	IC-PWR,VREG,SM,TSOT23-8,STEP DOWN,6V,2A,RICHTEK,RT5785C QUAL	VR_1P1STBY_RT

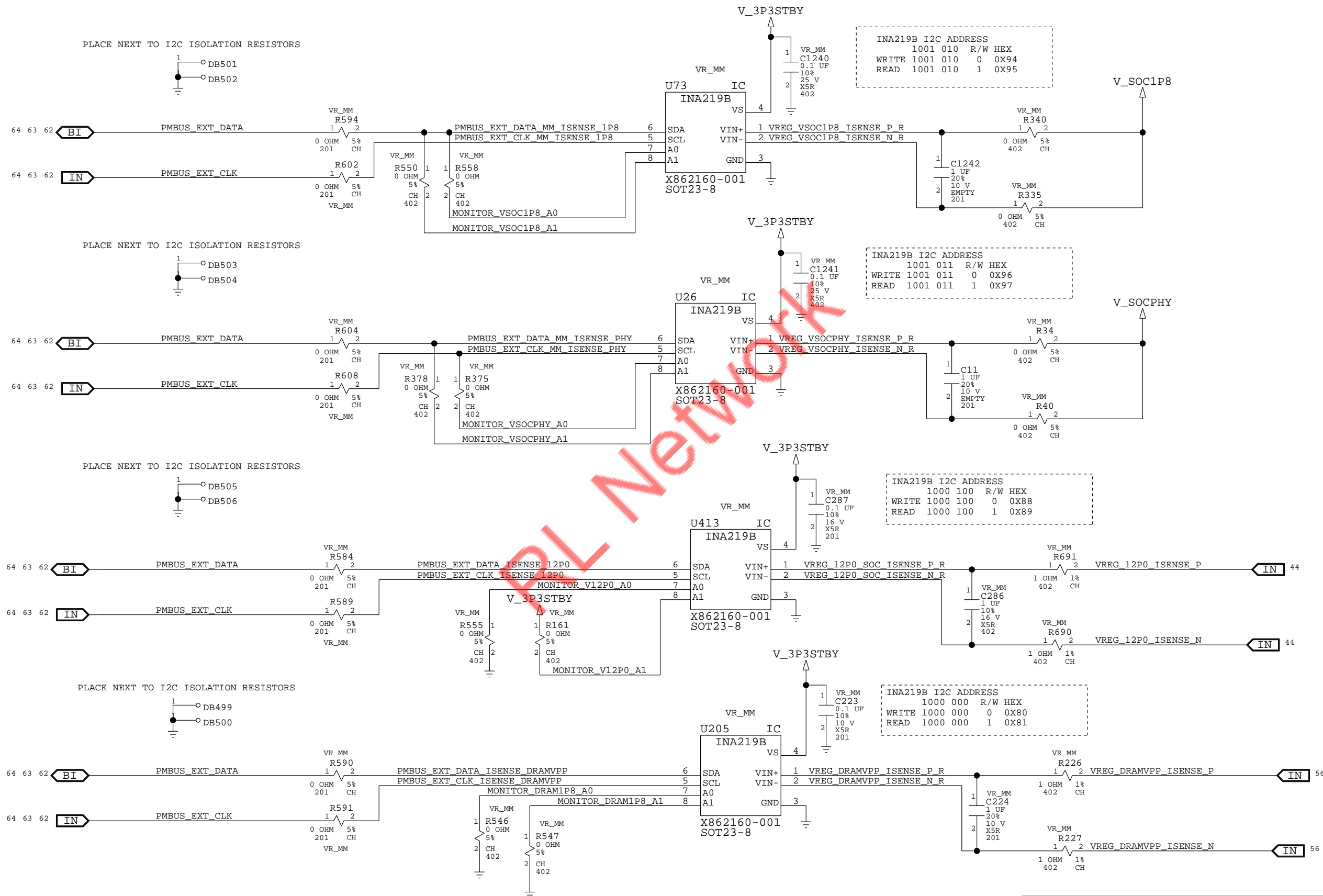
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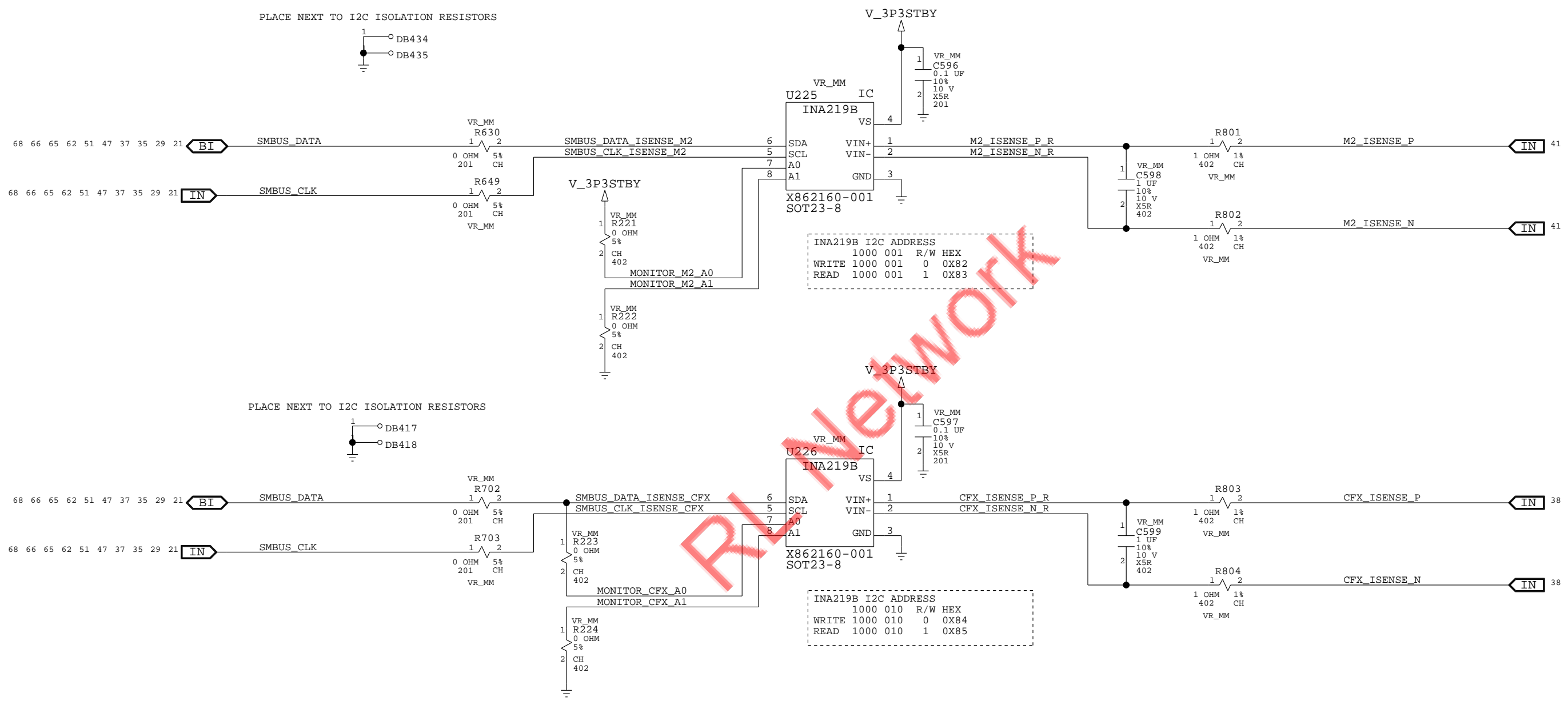
```
DEBUG: MARGIN V_SOCPHY,V_SOC1P8, V_DRAM1P8
```



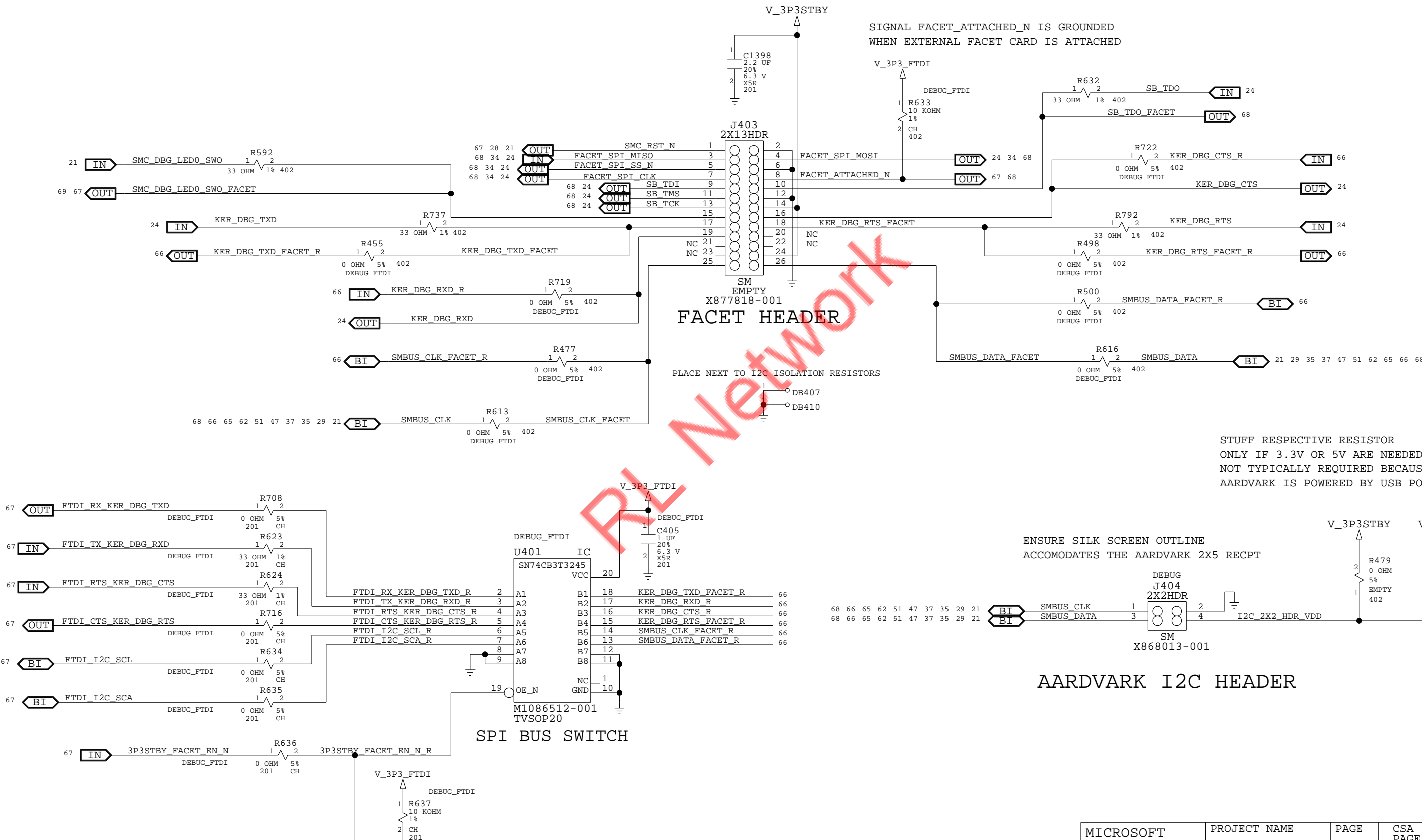
DEBUG: MONITOR V_SOC1P8, V_SOCPHY, V_12P0, V_DRAM1P8



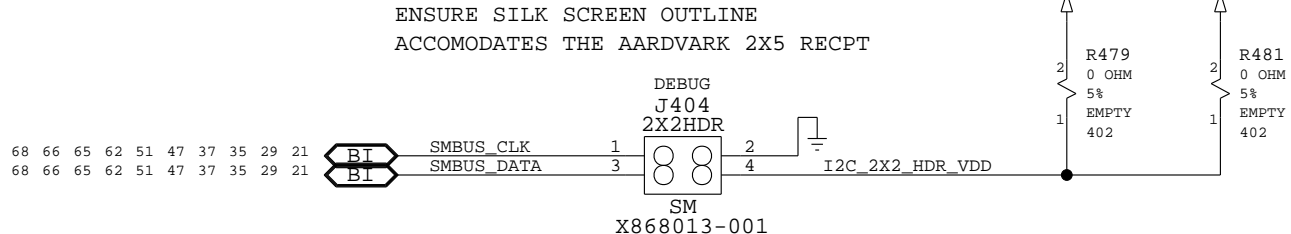
DEBUG: MONITOR M.2. CFEXPRESS



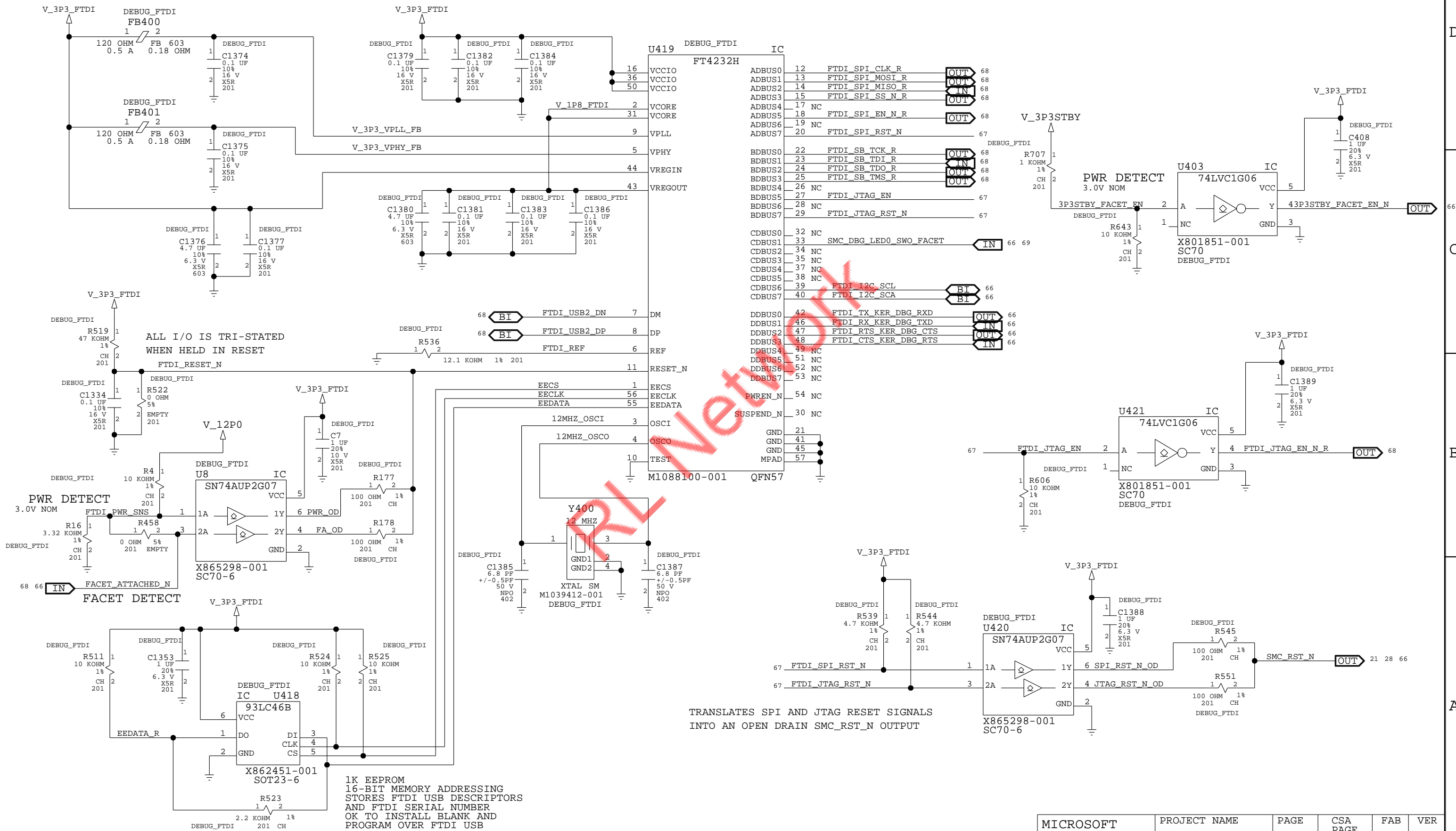
DEBUG: FACET HEADER

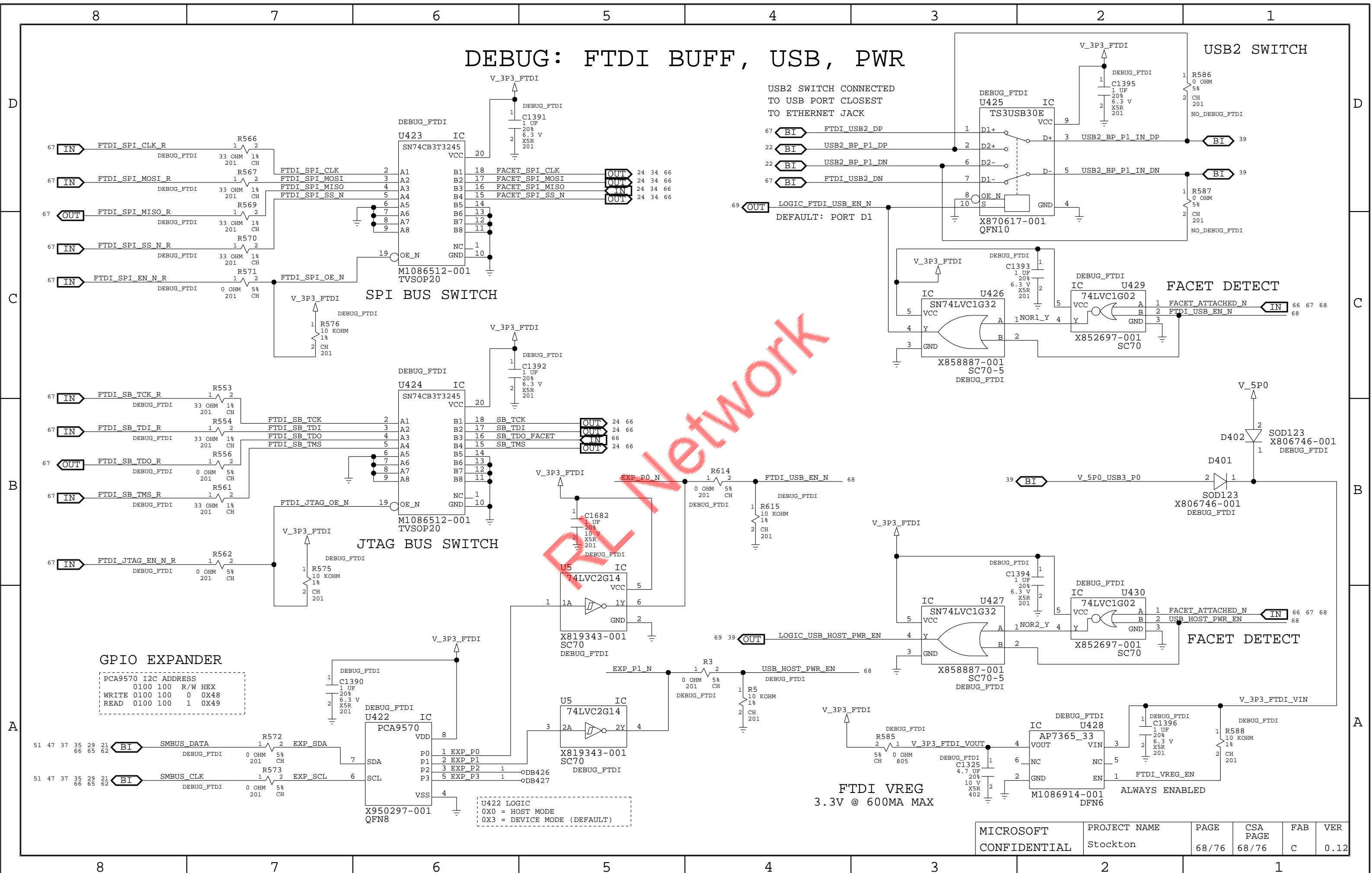


AARDVARK I2C HEADER

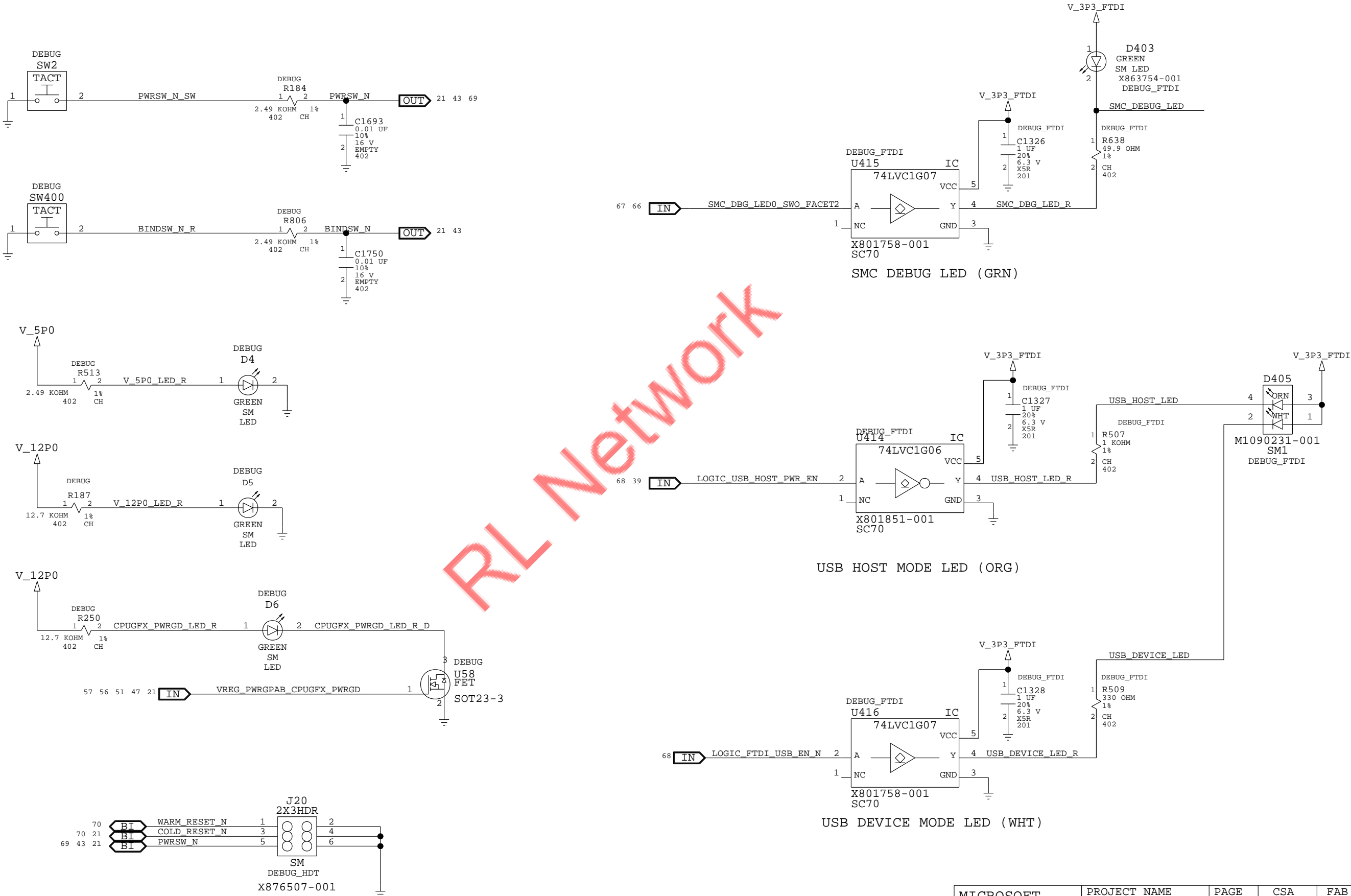


DEBUG: FTDI BRIDGE

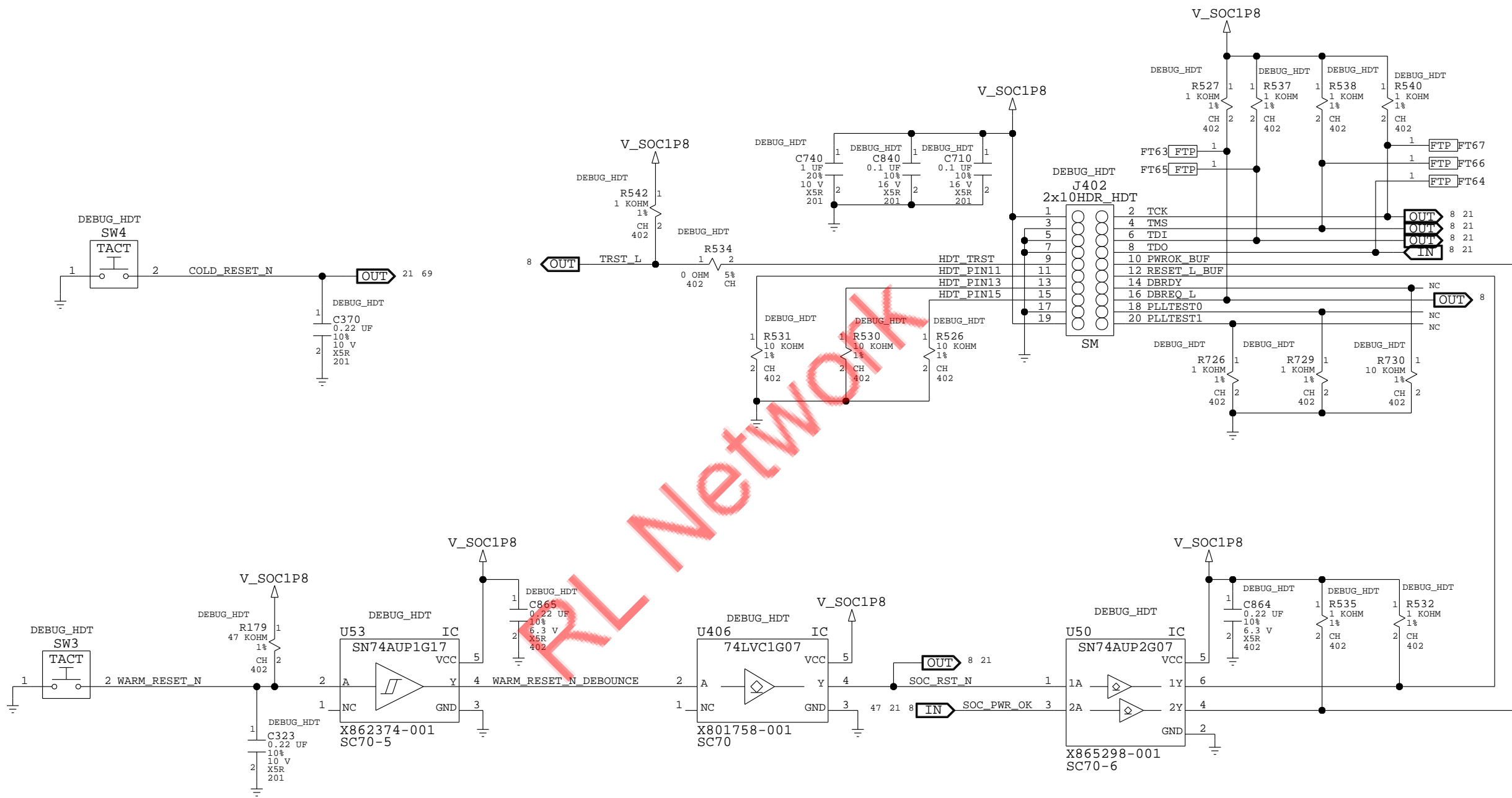




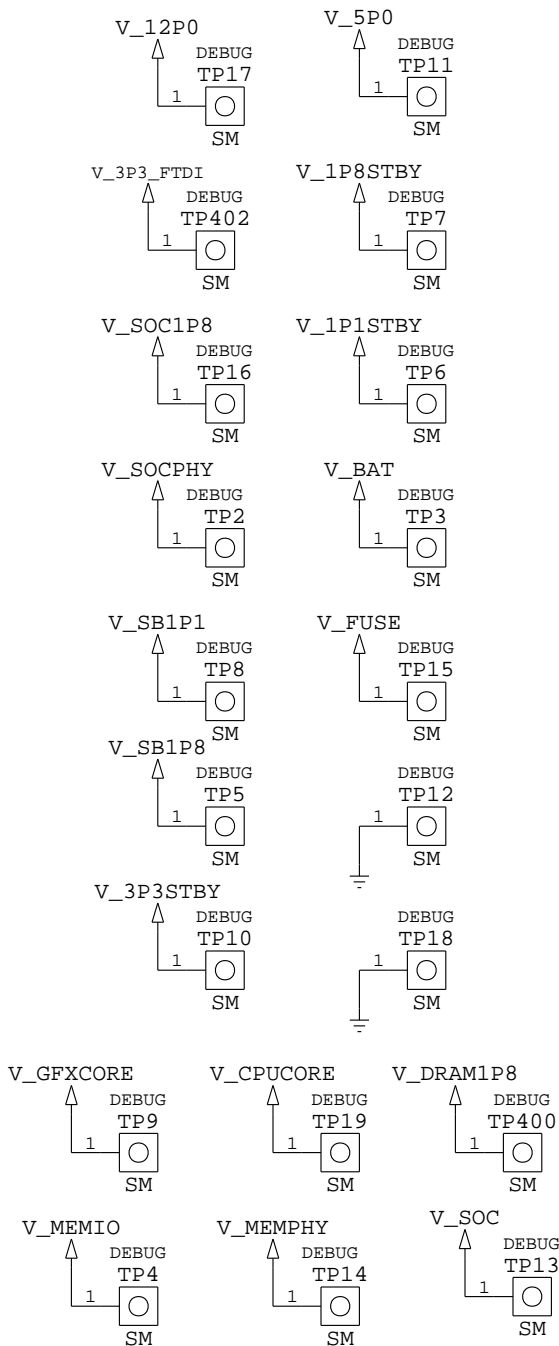
DEBUG: SWITCHES, LEDS



DEBUG: HDT

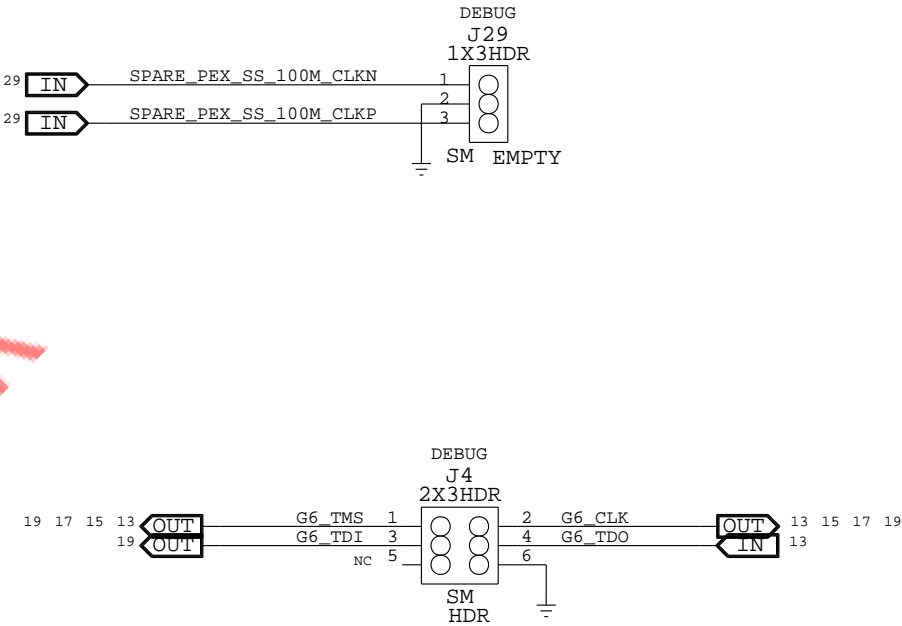


DEBUG: VR HEADERS, TEST POINTS, CONNECTORS



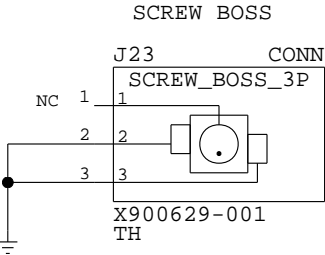
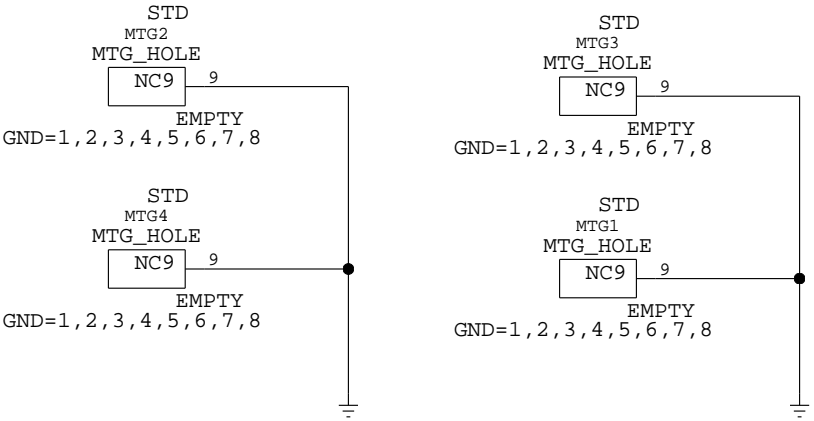
NOTE: THESE TEST POINTS ARE NOT
TO BE USED FOR VOLTAGE REGULATOR
QUALIFICATION TEST POINTS

PCIE CONNECTORS

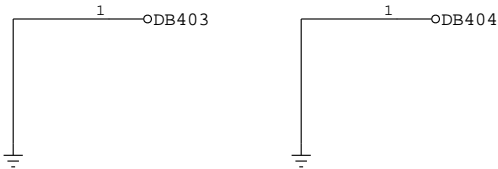


LABELS AND MOUNTING

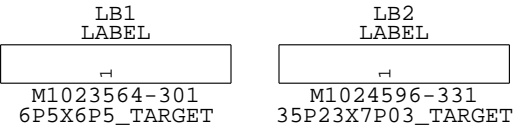
HEAT SINK MOUNTING HOLES



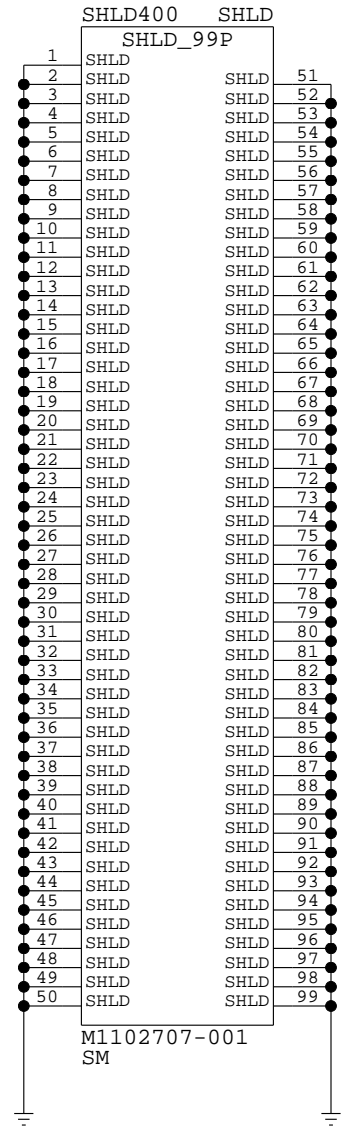
GND PADS FOR HEATSINK ALIGNMENT PINS



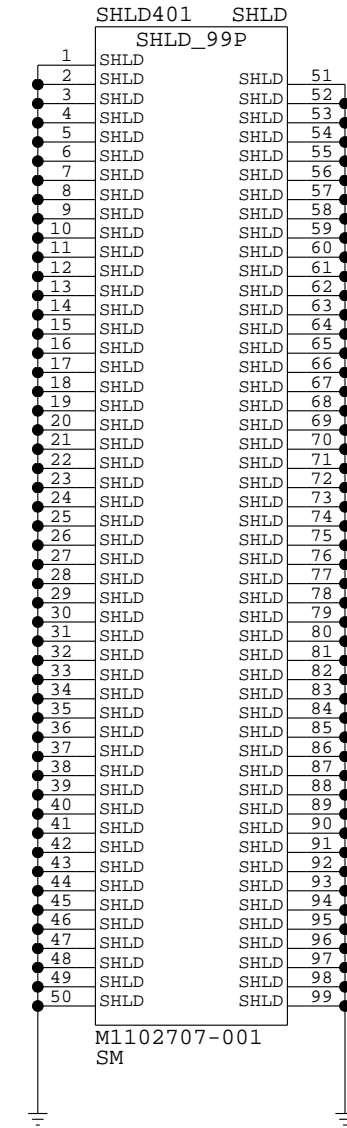
INTELLIGENT SERIAL NUMBER TARGET



TOP BOARD LEVEL SHIELD

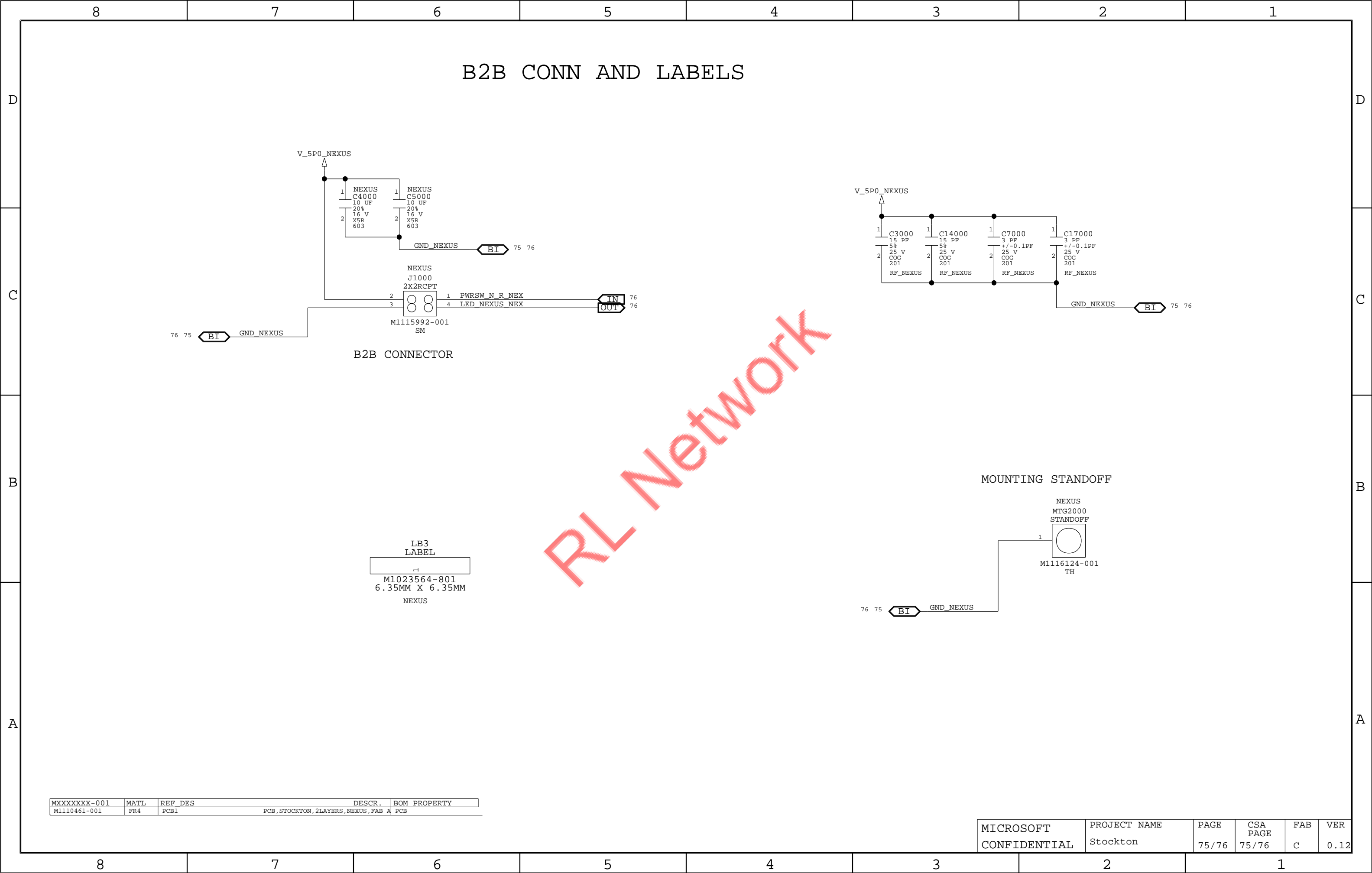


BOTTOM BOARD LEVEL SHIELD



MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
M1111890-001	FR4	PCB1	PCB, STOCKTON, FAB B, 8 LAYERS, GI	PCB_GI
MXXXXXXX-001	FR4	PCB1	PCB, STOCKTON, FAB B, 8 LAYERS, OSP	PCB_OSP

8		7		6		5		4		3		2		1		
BOM DEFINITIONS																
D	BOM		DEFINITION													
	AUDIO		INCLUDES COMPONENTS FOR THE STANDARD AUDIO SOLUTION													
	AUDIO_PREM		INCLUDES COMPONENTS FOR THE PREMIUM SE/LE SPEAKER SOLUTION													
	COMMON		ALL COMPONENTS WITH NO BOM PROPERTY													
C	DEBUG		COMPONENTS REQUIRED FOR BRING UP & DEBUG													
	DEBUG_HDT		HDT-RELATED DEBUG COMPONENTS													
	DEBUG_SHUNT		COMPONENTS WHICH ARE ON DEBUG BOARDS, BUT ARE REMOVED/SHORTED ON RETAIL													
	EMMC_BASE		DUMMY PLACE HOLDER FOR EMMC DEVICE & RESISTORS. NEVER USE THIS IN THE RECIPE FILE. SELECT ONE OF THESE INSTEAD: EMMC_HYNIX_16NM, EMMC TOSHIBA_15NM, EMMC SAMSUNG_14NM													
	EMMC_HYNIX_16NM		HYNIX EMMC DEVICE													
	EMMC_SAMSUNG_14NM		SAMSUNG EMMC DEVICE													
	EMMC_TOSHIBA_15NM		TOSHIBA EMMC DEVICE													
	SANTO_BASE		DUMMY PLACE HOLDER FOR SANTO SB. NEVER USE THIS IN THE RECIPE FILE. USE ONE OF THESE INSTEAD: SANTO_DEV OR SANTO_RETAIL													
	SANTO_DEV		DEBUG VERSION OF SANTO SB													
	SANTO_RETAIL		RETAIL VERSION OF SANTO SB													
	M2_ONLY		POPULATE TO SUPPORT AN M.2 INTERFACE													
	NO_M2		POPULATE WHEN THERE IS NO M2. INTERFACE													
B	PCB_GI		FAB TYPE: GOLD													
	PCB_OSP		FAB TYPE: ORGANIC SOLDERABILITY PRESERVATIVE GREEN SOLDERMASK													
	PCB_OSP_BLACK		FAB TYPE: ORGANIC SOLDERABILITY PRESERVATIVE BLACK SOLDERMASK													
	RTC_RETAIL		RTC CIRCUIT IMPLEMENTATION FOR RETAIL BOARDS													
	RTC_XDK		RTC CIRCUIT IMPLEMENTATION FOR XDK BOARDS													
	SOC_BASE		DUMMY PLACE HOLDER FOR SOC. NEVER USE THIS IN THE RECIPE FILE. SELECT ONE OF THESE INSTEAD: EMMC_HYNIX_16NM, EMMC TOSHIBA_15NM, EMMC SAMSUNG_14NM													
	SOC_EMPTY		DOES NOT STUFF SPARKMAN													
	SOC_INCLUDE		STUFFS SPARKMAN													
	VR_FIXED		SET ALL VRS TO FIXED VOLTAGES (NON-MARGINED). EXCLUDES V_MEMIO. MUST BE USED IN CONJUNCTION WITH NOT VR_MM													
	VR_MM		ALLOWS MOST VRS TO BE MARGINED FOR M&M BOARDS. EXCLUDES V_MEMIO. MUST BE USED IN CONJUNCTION WITH NOT VR_FIXED													
	RETAIL		COMPONENTS STUFFED FOR A RETAIL CONSOLE. DO NOT USE WITH DEBUG													
	DEBUG_PHASE		PHASES USED FOR INITIAL POWER UP													
A	DRAM_VPP_DEBUG		SEPARATES SOC 1.8V AND DRAM 1.8V. USE IF MARGINING SOC 1.8V OUTSIDE OF DRAM 1.8V LIMITS. NEVER USE WITH DRAM_VPP_RETAIL													
	DRAM_VPP_RETAIL		COMBINES SOC 1,8V AND DRAM1.8V USEING A FILTER NETWORK. NEVER USE WITH DRAM_VPP_DEBUG													
	DEBUG_FTDI		STUFFS INTERCEPT CIRCUITRY FOR DEBUG													
	NO_DEBUG_FTDI		BYPASSES INTERCEPT CIRCUITRY FOR NO DEBUG													
	SPI_FLASH_BASE		DUMMY PLACE HOLDER FOR SPI FLASH. NEVER USE THIS IN THE RECIPE FILE.													
	SPI_FLASH_MACRONIX		STUFFS MACRONIX SPI FLASH													
	SPI_FLASH_WINBOND		STUFFS WINBOND SPI FLASH													
8		7		6		5		4		3		2		1		
												MICROSOFT CONFIDENTIAL	PROJECT NAME Stockton	PAGE 73/76	CSA PAGE 73/76	VER 0.12



NEXUS LED AND POWER SWITCH

POWER SWITCH

NEXUS LED LIGHTING

